Ultimately Thin Double-Gate SOI MOSFETs

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***Abstract*—The operation of 1–3 nm thick SOI MOSFETs, in double-gate (DG) mode and single-gate (SG) mode (for either front or back channel), is systematically analyzed. Strong interface coupling and threshold voltage variation, large influence of substrate depletion underneath the buried oxide, absence of drain current transients, degradation in electron mobility are typical effects in these ultra-thin MOSFETs. The comparison of SG and DG configurations demonstrates the superiority of DG-MOSFETs: ideal subthreshold swing and remarkably improved transconductance (consistently higher than twice the value in SG-MOSFETs). The experimental data and the difference between SG and DG modes is explained by combining classical models with quantum calculations. The key effect in ultimately thin DG-MOSFETs is volume inversion, which primarily leads to an improvement in mobility, whereas the total inversion charge is only marginally modified.**

***Index Terms*—Double gate, mobility, MOS transistor, MOSFET, SOI, thin film.**

I. INTRODUCTION

THE silicon on insulator (SOI) technology is extremely attractive in terms of performance (high speed, low power consumption, radiation-hard) and advanced scalability [1]. As compared to bulk silicon, the architecture of SOI MOSFETs is more flexible because more parameters—such as thicknesses of film and buried oxide, substrate doping, and back gate bias—can be used for optimization and scaling. It is well known that the short-channel effects are remarkably reduced in ultra-thin SOI films [1]–[9]. 50 nm long MOSFETs were already processed on 2–6 nm SOI films [10]. But what are exactly the meaning and the limits of an “ultra thin” film? We will demonstrate in Section II that transistors with a 1nm-thick body can be fabricated and operated successfully.

A direct application of these extremely thin films is the double-gate transistor (DG-MOSFET), which makes use of the *volume inversion* concept formulated, in 1987, by Balestra *et al.* [11]. Recently, these devices have received considerable attention from the viewpoint of their technological feasibility and theory. Several approaches for the device architecture have been explored: gate-all-around (GAA) [7], Delta [12], lateral epitaxial overgrowth [13], [14], folded-gate [15], Fin-gate [16], self-alignment [17] etc. Electrostatic and Monte-Carlo simulations have demonstrated the advantage of DG-MOSFETs down to 10 nm and below [9], [18], [19]. Impressive compact and analytical models for DG-MOSFETs, which account for quantum, volume-inversion, short-channel, and nonstatic effects have been proposed in [20], [21]. Thanks to the excellent control of the potential, it is admitted that DG-MOSFETs will presumably represent the final stages of the Si microelectronics [6], [9], [18], [20].

Starting from this postulate, our work is focussed on extreme thickness effects. We first compare the experimental characteristics and performance of single-gate (SG) and double-gate (DG) SOI MOSFETs (Section III). Although the transistors are long, a clear advantage is observed for DG-MOSFETs, which is discussed in Section IV, based on self-consistent quantum calculations. The benefits of volume inversion are evaluated in terms of total charge, average vertical field, and effective mobility.

II. TRANSISTOR FABRICATION

N-channel MOSFETs were fabricated at the NTT laboratories (Japan) on low-dose SIMOX wafers; the buried oxide (BOX) is 62 nm thick. The transistor body, left undoped (initial doping: $N_A \simeq 5 \times 10^{14}$ cm^{-3}), was thinned down to 1–6 nm by sacrificial oxidation. The cross-section of a 3-nm-thick SOI film is shown in Fig. 2(a). The film thickness was measured by ellipsometry and interferometry with ±0.5 nm accuracy. The control of the thickness uniformity is very difficult. In particular, 1-nm-thick MOSFETs contain Si holes leading to “swiss-cheese” effects: the effective length is increased (because electrons have to bypass Si holes) while the effective width is strongly reduced.

The source and drain terminals are much thicker (elevated structures) which allows maintaining reasonable source and drain series resistances. To minimize the influence of the device topology, only long channels (from 3 to 30 μm) have been fabricated. Double-gate operation requires quasi symmetrical front and back gate oxides. Since the BOX cannot be thinned aggressively, a thick gate oxide (50 nm) has been grown instead.

III. SINGLE-GATE AND DOUBLE-GATE OPERATION

A. Front-Channel Characteristics

Typical front-channel current $I_D(V_{G_1})$ curves are shown for a 1-nm-thick record transistor in Fig. 1. In spite of the fact that only 3–4 mono-layers of silicon are involved, the characteristics are still MOS-like and well behaved. We therefore expect that the MOS “gene” can be transmitted further down to 1–2 atoms of Si.

Moreover, since the characteristics look pretty conventional, it follows that standard techniques can be applied for the param-

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