Silicon-on-Nothing MOSFETs: Performance, Short-Channel Effects, and Backgate Coupling

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***Abstract*—Silicon-on-nothing (SON) transistors with gate length varying from 0.25 μm down to 80 nm exhibit excellent performance and scalability. The silicon-on-insulator (SOI)-like architecture with thin fully depleted Si film and ultrathin buried oxide results in attenuated short-channel effects (charge sharing, DIBL and fringing fields), high current, and electron mobility. A new model accounts for the intrinsic mechanisms of operation in SON MOSFETs: i) substrate depletion governed by source and drain via doping modulation, ii) relatively low coupling between the front- and backgates, iii) role of ultrathin buried oxide. The proposed model reproduces the variations of the threshold voltage and subthreshold swing and is useful for further device optimization.**

***Index Terms*—Doping modulation, interface coupling, short-channel effects, silicon-on-insulator (SOI) MOSFETs, silicon-on-nothing (SON) technology.**

I. INTRODUCTION

SHORT-CHANNEL EFFECTS (SCEs), transistor scalability, and circuit performance are improved by using silicon-on-insulator (SOI) technology, especially ultrathin, fully depleted (FD) MOSFETs [1]. Their development has been limited so far by the difficulty in controlling the silicon film thickness, the series resistances, and the fringing fields [2]–[4]. Silicon-on-nothing (SON) technology has been proposed as an alternative solution for advanced scaling [5], [6]. It combines the advantages of FD-MOSFETs (excellent subthreshold slope and mobility, no floating-body effects, ...) with those of bulk silicon (lower series resistances and better heat dissipation) [7]–[9]. In addition, SON provides a good control of the silicon film thickness, fringing fields, and halo profiles which are basic ingredients for advanced scalability.

Preliminary results showing the good drivability of SON transistors have been reported recently [10]. In this paper, we examine for the first time a number of special properties and mechanisms of SON MOSFETs. SCEs are analyzed in terms of charge sharing, drain-induced barrier lowering (DIBL), and fringing fields. On the other hand, backgate bias experiments demonstrate that SON transistors operate in full depletion mode, with attenuated coupling between the front and back interfaces. We propose a new coupling model, which is necessary to take into account the specifics of the SON structure: very thin buried oxide (BOX), two active BOX interfaces, and substrate depletion controlled by source and drain. The new model includes the concept of voltage doping transformation and accurately describes the behavior of the threshold voltage and the subthreshold swing.

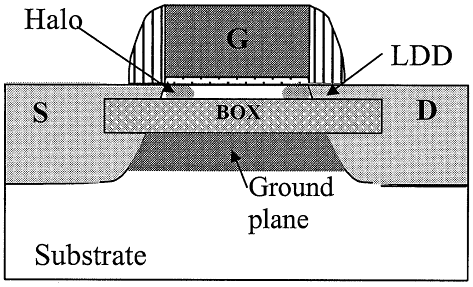

Fig. 1. Schematic architecture of a SON MOSFET.

II. DEVICE PROCESSING

The SON process [5] consists of growing a sacrificial SiGe layer on which a Si film is epitaxially grown. Removing the SiGe layer leaves an empty space (air-gap or tunnel) underneath the film (i.e., SON). The subsequent process results in an ultrathin (25 nm) buried insulator (BOX) with multilayer and multi-interface configuration: i) during thermal oxidation, two oxide layers are formed on each side of the air-gap, ii) HTO adds two more oxide layers, iii) two nitride layers are grown for refilling the tunnel.

N-channel MOSFETs had a body doping of $N_A \approx 2\ 10^{18}$ cm^{-3}, a gate-oxide thickness of 3 nm, and a Si-film thickness of 20 nm. The gate length varied from 0.25 μm to 80 nm and the channel width was 10 μm. Local epitaxy was performed to raise the source and drain terminals. To prevent punchthrough, the substrate was doped underneath the BOX (i.e., ground plane concept, Fig. 1).

III. MEASUREMENTS AND ANALYSIS

A. Typical Performance and SCEs Due to Charge Sharing

The threshold voltage V_T, subthreshold swing S, and low-field mobility μ were chosen as main parameters to evaluate the capability of SON MOSFETs. The length-dependent values of V_T and μ were extracted from the experimental data by using the function $Y(V_G) = I_D/\sqrt{g_m}$ (g_m being the transconductance and I_D the drain current). This procedure eliminates first order effects of series resistance and mobility reduction at high fields [11].

Manuscript received April 24, 2003; revised September 17, 2003. The review of this paper was arranged by Editor R. Shrivastava.

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Digital Object Identifier 10.1109/TED.2003.822226