ADJUSTABLE CONFINEMENT OF THE ELECTRON GAS IN DUAL-GATE SILICON-ON-INSULATOR MOSFET's

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The confinement of the electron gas in MOS structures fabricated on thin silicon on insulator (SOI) layers is studied with emphasis on the principle of volume inversion. Analytical solutions are proposed for the potential distribution across the film and energy quantization. It is found that the triangular potential well approximation, which holds in bulk Si MOS systems, is no longer valid in SOI. Instead, the potential becomes parabolic, and even rather flat for SOI films which are very thin ($30 - 100\ nm$) and not intentionally doped ($10^{15}\ cm^{-3}$). The energy separation of the lowest subbands is extremely small so that the quantum effects can be ignored. This confirms that the minority carriers are absolutely free in the volume of the film, their distribution being totally governed by the Poisson equation and current conservation equation. The presence of the natural back gate in SOI-MOS structures makes possible not only the volume inversion or accumulation but also the transition from 3-D to 2-D systems.

1. Introduction

Silicon On Insulator (SOI) materials are currently under intense investigation for the fabrication of advanced integrated circuits with unique properties : full isolation, reduced parasitic capacitances, vertical junctions, high speed, reduced hot carrier injection and short channel effects, simpler design and excellent tolerance to radiation effects. An SOI structure consists of a thin monocristalline Si film (t_s = 50-300 nm), separated from the bulk Si substrate by a buried SiO_2 layer (t_b = 200-1000 nm). Several methods are competitively developed for the synthesis of SOI substrates [1] : deep implantation of high doses of oxygen (SIMOX), recrystallisation of poly-Si films deposited on SiO_2, oxidation of porous Si and wafer bonding.

Many important features of the MOS transistors fabricated on SOI (Fig.1) result from the dual-gate control of the electrostatic potential in the Si island.

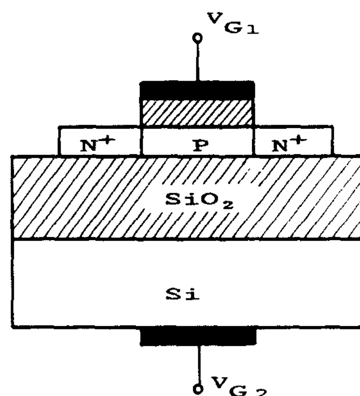

Fig.1. *Schematic diagram of an enhancement-mode SOI-MOS transistor.*

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