

# Optimization of SIMOX for VLSI by Electrical Characterization

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**Abstract**—A comprehensive electrical characterization study was conducted to optimize the fabrication of SIMOX substrates for VLSI. The oxygen implantation was carried out using medium-current and high-current implanters and the wafers were annealed at 1275°C and 1300°C to produce high-quality, precipitate-free material. The sample selection was designed to study three main aspects of this technology: the effect of dose, the effect of multiple implantation (by sequentially implanting and annealing), and the effect of anneal ambient gas and capping layer during annealing. MOSFET's of various geometries and gate oxide of ~20 nm were fabricated by a CMOS process incorporating the addition of a thin epitaxial Si layer. A general evaluation of each transistor was conducted by studying its static  $I_D(V_G, V_D)$  characteristics. The interface states were evaluated by dynamic conductance, dynamic transconductance, and charge pumping; the bulk traps by current-DLTS; and carrier generation phenomena by generation-DLTS and the dual-gate Zerbst-like method. Good-quality interfaces were obtained, in particular by a relatively low oxygen dose ( $1.4 \times 10^{18} \text{ cm}^{-2}$ ) and high-temperature annealing ( $\geq 1275^\circ\text{C}$ ); better implantation control reduced contamination and suppressed deep traps below the detection limit; and multiple implantation resulted in superior material quality, as evidenced by very long generation lifetime values ( $> 100 \mu\text{s}$ ).

## I. INTRODUCTION

THE advantages of silicon-on-insulator (SOI) CMOS technology and in particular of thin-film SOI are well known [1]. SIMOX (Separation by IMplanted OXYgen) [2] is currently the leading technology for the fabrication of SOI substrates. This involves implanting a high dose of energetic oxygen ions (typically  $1\text{--}2 \times 10^{18} \text{ O}^+ \text{ cm}^{-2}$  at 150–200 keV) into a Si wafer at elevated temperatures (typically  $> 500^\circ\text{C}$ ), followed by high-temperature annealing (typically  $> 1250^\circ\text{C}$ ) [3]. The quality of the resulting substrate and devices made on it depends on the implantation conditions (energy, dose, current, temperature, screen), and post-implantation treatments. Whereas much work was done in the past with low-current implanters ( $< 1 \text{ mA}$ ), most SIMOX substrates are currently made with high-current implanters (100-mA class). The subject has been intensively

studied in the last few years and various conditions for obtaining good-quality materials and devices have been described [4]–[16]. The present study is aimed at taking a more detailed look at some of the factors involved by combining a multitude of techniques to characterize the channel mobility, interface quality, deep traps, and carrier generation in CMOS transistors made on a variety of SIMOX substrates.

## II. SAMPLE SELECTION

It has now been established that high-temperature annealing (HTA) above  $\sim 1250^\circ\text{C}$  for several hours is required in order to obtain high-quality, precipitate-free SIMOX substrates [7], [8]. The wafers studied in this work were therefore annealed at 1275°C and 1300°C. A medium-current (10-mA class) and a high-current (100-mA class) implanter were used to carry out the oxygen implantations. Ion beam heating was used to keep the wafer temperature during implantation at  $T_i \approx 550^\circ\text{C}$  and  $T_i \approx 650^\circ\text{C}$ , respectively, [4], [9]. The medium-current implantations were made through a thin dioxide layer, previously deposited on the wafer (screen oxide); no screen oxide was used for the high-current implantations.

The sample selection was designed to study the following three main aspects of this technology: the effect of dose (wafers MD2A, B, C), the effect of ambient gas and capping layer during annealing (MD5 and MD6A, B), and the effect of multiple implants by sequentially implanting and annealing (MD11). The starting material was (100) n-type (MD2A, B, C) or p-type (MD5, MD6A, B, and MD11) silicon wafers with resistivity  $\sim 5 \Omega \cdot \text{cm}$ . Wafers MD2A, B, and C were implanted at energy 150 keV with dose 1.4, 1.8, and  $2.1 \times 10^{18} \text{ O}^+ \text{ cm}^{-2}$ , respectively, and annealed at 1275°C in nitrogen. Wafers MD5, MD6A, and MD6B were implanted at energy 175 keV with dose  $1.8 \times 10^{18} \text{ O}^+ \text{ cm}^{-2}$  and annealed at 1275°C, MD5 in nitrogen, and MD6A and B in argon. MD6A had in addition a  $\text{SiO}_2$  layer deposited on the surface prior to annealing (cap layer). Finally, wafer MD11 was multiply implanted to a total dose of  $1.5 \times 10^{18} \text{ O}^+ \text{ cm}^{-2}$  in three steps of  $0.5 \times 10^{18} \text{ O}^+ \text{ cm}^{-2}$ , where each implantation step was followed by annealing at 1300°C in argon for 6 h using a  $\text{SiO}_2$  cap. Both the nitrogen and argon annealing ambients were made partially oxidizing by adding a small amount of oxygen ( $\sim 1\%$ ) to preserve surface integrity. The details of the fabrication of the above SIMOX wafers are summarized in Table I, where it is seen that the duration of the annealing was sufficient to produce precipitate-free material [7], [8] in all cases. Finally, MOSFET's of various geometries were fabricated by a standard CMOS process [9], incorporating a thin silicon epitaxial layer and threshold and doping adjustment implants. The total silicon film in the finished devices was 0.34  $\mu\text{m}$  thick and fairly uniformly doped p-type, the dopand con-

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