



Electron transport in silicon-on-insulator devices

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Abstract

The electron transport in single-gate and double-gate silicon-on-insulator devices is studied as a function of the transverse electric field and the silicon layer thickness, with particular attention to the evaluation of stationary drift velocity and low-field mobility at room temperature. © 2001 Elsevier Science Ltd. All rights reserved.

1. Introduction

In recent years, many techniques to enhance the carrier mobility in metal-oxide-semiconductor-field-effect-transistor (MOSFET) channel have been examined [1]. We can mention, for example, the use of specific doping profiles [2], the growth of low doped epitaxial layers on high doped substrates [3] or even the use of other materials instead of silicon [4]. With reference to the use of other materials, it has very recently been shown that one way of increasing electron mobility lies in employing strained silicon to build the MOSFET channel [5]. Recently, both theoretical and experimental studies have shown spectacular electron mobility enhancement when silicon is grown pseudomorphically on relaxed $\text{Si}_{1-x}\text{Ge}_x$ at different temperatures. Another example is the use of ultrathin silicon-on-insulator (SOI) devices [6]. SOI technology has great potential for future electronic technology because of the many advantages that these devices present compared to their bulk counterparts, and because of its compatibility with existing fabrication facilities [7]. Although a great deal of work has been done during the last few years to study the carrier transport properties of these devices many questions remain open. In this paper we summarize the

main results we have obtained on the transport properties of electrons in single-gate (SG) and double-gate (DG) devices [8–11].

2. Single-gate silicon-on-insulator devices

The first structure studied is a SGOI MOSFET. This device consists of an undoped (100)-silicon film sandwiched between two oxide layers. The gate-oxide thickness was taken as 5 nm, while the buried oxide was considered to be 80 nm thick. A silicon substrate was assumed under the buried oxide. A P^+ poly gate was employed (Fig. 1a). Different thicknesses of the silicon film, T_w , were considered.

2.1. Poisson–Schroedinger solution

To accurately evaluate the electron distribution in these structures we must self-consistently solve the Schroedinger and Poisson equations. To solve Poisson's equation we have considered a non-uniform adaptive mesh, employing an iterative-Newton scheme. The actual band bending through the whole structure and the finite height of the barrier at the Si– SiO_2 interfaces have been considered. A simple non-parabolic band model for the silicon has been taken into account assuming $\alpha = 0.5$ eV, α being the parameter of non-parabolicity. This limits our study to low-electron energies (below 0.5 eV) [12].

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