

New SOI lateral power devices with trench oxide

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Abstract

We describe new SOI lateral power devices which have a trench oxide to improve the device performance. High-voltage super-junction (SJ) SOI-LDMOSFETs have a trench oxide in the drift region. It allows to reduce the drift length without degrading the breakdown voltage. With the proposed device structure a reduction of the on-resistance of the *n*-drift layer can be achieved. The breakdown voltage and the specific on-resistance of the suggested devices as a function of the trench oxide depth, the *p*-column width, and the doping are studied. Shorted-anode lateral insulated-gate bipolar transistors (SA-LIGBTs) on SOI have a trench oxide at the drain/anode region. It suppresses effectively the snap-back voltage inherent in conventional SA-LIGBTs without increasing the anode length of the device. Using the two-dimensional numerical simulator *Minimos-NT*, we confirm that the drift length of the proposed SJ SOI-LDMOSFETs is reduced to 65% compared to conventional devices, and a weak negative differential resistance region is observed with the proposed SOI SA-LIGBT.

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1. Introduction

Lateral power devices on SOI (silicon on insulator) have attracted much attention in a wide variety of applications such as automotive electronics, consumer electronics, telecommunications, and industrial electronics [1]. Advantages of SOI technology are superior isolation, reduced parasitic capacitances and leakage currents, and superior high temperature performance compared to traditional junction isolation. These advantages allow efficient monolithic integration of multiple power devices and low-voltage control circuitry on a single chip. The main issues in the development of these devices are to obtain the best trade-off between the specific on-resistance (R_{SP}) and the breakdown voltage (BV) [2], and to shrink the feature size without degrading device characteristics. In order to fulfill these requirements new structures such as super-junctions [3], buried gate oxide

devices [4], LUDMOSFETs [5], trench lateral power MOSFETs with a trench bottom source contact (TLPM/S) [6], the multi-channel approach [7], and hybrid SOI LDMOS-IGBT [8] have been proposed. Vertical SJ devices such as COOLMOS [9] and MDmesh [10] assume complete charge balance of the depletion layer. This can be achieved by introducing alternating *n*- and *p*-columns in the drift region, which allow to drastically increase the doping in this region. This results in a significant reduction in R_{SP} of the devices. Recently a lateral SJ SOI-LDMOSFET [11] which has a channel on the side wall of the device was proposed to improve on-state characteristics. The channel can be made by a lateral trench gate, which increases the channel area.

To obtain the best trade-off between R_{SP} and BV, we suggest a SJ SOI-LDMOSFET which has an extra *p*-column and a trench oxide in the drift region. The extra *p*-column is doped to achieve a balanced charge condition which means that the net depletion layer charge is zero. The trench oxide in the *p*-column helps to reduce the drift length without further decreasing the conduction area (only the *n*-column contributes to the current conduction). The R_{SP} of the proposed structure is

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