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Electron mobility in ultrathin silicon-on-insulator layers at 4.2 K

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Low temperature mobility measurements of silicon-on-insulator (SOI) metal-oxide-field-effect-transistors are reported. The batch of devices fabricated in this work includes both ultrathin and thick devices for which the SOI film thicknesses are in the ranges of 10–15 nm and 56–61 nm, respectively. The 4.2 K peak mobility of the thick devices is 1.9 $\mathrm{m}^2/\mathrm{V\,s}$. The ultrathin devices show mobility degradation at low electron densities where the mobility is also observed to decrease with decreasing the SOI film thickness. The peak mobilities of these devices are in the range of 1.35–1.57 $\mathrm{m}^2/\mathrm{V\,s}$. Numerical calculations show that ultrathin devices are in the limit where the electrons are confined by the quantum well defined by gate oxide and buried oxide, which is interpreted to lead to the observed mobility degradation. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1687980]

Mobility of the quasi two-dimensional (2D) electron system in the inversion layer of a bulk silicon metal-oxide-semiconductor-field-effect-transistor (MOSFET) is defined by the scattering phenomena arising from electron interaction with phonons, Si–$\mathrm{SiO_2}$ interface roughness and Coulomb centers.[1,2] The understanding of the underlying physics of these phenomena is relatively well established. However, the availability of very high mobility samples has created a new branch to the fundamental Si inversion layer physics which studies the metallic phenomena at low electron concentrations and temperatures.[3] Another interesting branch of Si inversion layer physics has emerged with the silicon-on-insulator (SOI) technology. SOI has also a large technological and commercial impact due to many advantages and full process compatibility in comparison with the current Si-based technology.[4] As SOI MOSFETs are scaled down the SOI thickness should also be reduced to, e.g., alleviate short channel effects. From a physical point of view the utilization of very thin SOI in MOSFET devices changes the confinement of the carriers because the electron gas is sandwiched between the gate oxide and buried oxide (BOX) layers.[5] In addition, the proximity of the BOX layer is expected to alter the scattering phenomena. Some experimental and theoretical work has already been reported on the effective room temperature mobility in extremely thin SOI MOSFETs.[6–9] In this letter we report on fabrication and detailed low temperature Hall mobility measurements of extremely thin SOI MOSFETs.

SOI MOSFET Hall bars with a $100\times1900\ \mu\mathrm{m}^2$ channel dimensions and a 400 μm voltage probe distance were fabricated on commercially available 100 mm unibond (100) SOI wafers produced by smart-cut process.[10] The nominal SOI film thickness was 340 nm and the buried oxide was 400 nm thick. The initial acceptor (boron) concentration of the SOI was $\sim10^{15}\ \mathrm{cm}^{-3}$. A large scale variation of ~5 nm of the SOI film thickness was already observable across the wafer before any process steps. The thickness fluctuation is probably due to the chemical-mechanical polishing step used in the smart-cut process.[10] This intrinsic large scale nonuniformity enables us to study the electronic properties of devices with slightly different channel thicknesses.

First, the SOI film was thinned by thermal oxidation and oxide stripping to a thickness of 180 nm. Then half of the wafer was covered by silicon nitride and the other half was further thinned utilizing local oxidation of silicon (LOCOS). A second LOCOS step was performed to locally reduce the thickness of the Hall bar channels. The Hall bar mesas were patterned by UV lithography and dry etching. After implanting the contact areas, a 41-nm-thick gate oxide was grown, followed by deposition of 250-nm-thick polysilicon gate. Finally, after patterning the Al bonding pads, the samples were annealed in $\mathrm{H_2/N_2}$ ambient at 425 °C for 30 min. The process resulted in two sets of devices on the same wafer with channel thicknesses ranging from 10 to 15 nm and from 56 to 61 nm, respectively.

Prior to growth of the gate oxide we mapped the SOI film thickness ($t_{\mathrm{SOI},0}$) by fitting theoretical reflectance to experimental scanning reflectance in a 480–800 nm wavelength range (~15 μm spot diameter). Each point of the film thickness data represented on the left vertical axis in Fig. 1(a) was measured with this procedure from the middle of the Hall bars. The final SOI film thickness (t_{SOI}) can be calculated from $t_{\mathrm{SOI},0}$ and gate oxide thickness, but to avoid possible systematic errors we fixed t_{SOI} [right vertical axis in Fig. 1(a)] by performing a high-resolution-transmission-electron-microscopy (HRTEM) analysis on one of the Hall bars. Figure 1(b) shows a cross-sectional HRTEM image of this device and from the figure we determined that final SOI thickness of the device is $t_{\mathrm{SOI}}\approx13$ nm. The TEM analysis also showed that the SOI film is highly uniform (on a scale of few 100 μm) and free from defects.

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