

Strained-Si/SiGe-on-insulator inversion layers: The role of strained-Si layer thickness on electron mobility

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We show by Monte Carlo simulation that electron mobility is greater when strained-silicon inversion layers are grown on SiGe-on-insulator substrates than when unstrained-silicon-on-insulator devices are employed (as experimentally observed). However, the electron mobility in strained-Si/SiGe-on-insulator inversion layers is strongly dependent on the strained-silicon layer thickness, T_{Si} , due to an increase of the phonon scattering, which partially counteracts the increase in the mobility achieved by the strain. This effect is less important as the germanium mole fraction, x , is reduced, and as the value of T_{Si} increases. © 2002 American Institute of Physics. [DOI: 10.1063/1.1483907]

Recent studies have shown the feasibility of strained-Si/SiGe-on-insulator (SiGe-OI) structures. Such studies have obtained high-quality crystalline relaxed SiGe layers with a thickness of less than 10 nm on SiO₂ substrates by separation-by-implanted-oxygen techniques,^{1,2} or by solid-phase epitaxy.³ Using these structures as a starting point, and growing a thin strained-silicon layer on the relaxed SiGe-OI substrate, both *n*- and *p*-channel strained-Si/SiGe-OI metal-oxide-semiconductor field-effect transistors (MOSFETs) have been fabricated and successfully operated, showing high electron and hole mobilities with a germanium mole fraction as low as 0.1.^{2,4} These strained-Si/SiGe-OI structures combine the advantages of strained-Si/SiGe bulk MOSFETs^{5,6} and those of ultrathin fully depleted silicon-on-insulator (SOI) MOSFETs,^{7,8} at the same time overcoming the deficiencies they present separately. Thus, this device seems like an ideal candidate for future complementary metal-oxide-semiconductor technology generations. Figure 1 illustrates this structure.

As is well known, the strain in the silicon layer causes the six-fold degenerate valleys of the silicon conduction band minimum to split into two groups: two lowered valleys with the longitudinal effective mass axis perpendicular to the interface, and four raised valleys with the longitudinal mass axis parallel to the interface. The combination of a lighter effective mass and reduced intervalley scattering gives rise to higher electron mobility,⁶ and originates spectacular electron velocity overshoot.⁵ In Si/SiGe-OI structures, these advantages are combined with the use of an insulating substrate: the resulting structure provides good control of short channel effects, lower parasitic capacitance, and higher radiation tolerance, as well as mobility values that are much higher than those found in conventional SOI MOSFETs. Nevertheless, to achieve these results, and also to provide a low off-state leakage current, to allow operation at low voltages, and to avoid the floating body effect, the Si/SiGe structure sandwiched between the two oxides must be thin enough ($T_w = T_{\text{Si}} + T_{\text{SiGe}} < 30$ nm),⁸ where T_{Si} and T_{SiGe} are the thick-

nesses of the strained-Si layer and of the relaxed SiGe layer, respectively. On the other hand, in order to maintain the strain, the silicon layer must be sufficiently thinner than the SiGe layer. Therefore, taking into account both conditions, ($T_w < 30$ nm and $T_{\text{Si}} < T_{\text{SiGe}}$), the strained-silicon layer thickness has to be reduced to a very low value ($T_{\text{Si}} < 10$ nm). However, we have observed that when such thin strained-Si layers are used, the phonon scattering rate increases: the discontinuity of the conduction band at the Si/SiGe interface (as shown in Fig. 1), produces a greater confinement of the electrons, and therefore, a decrease in the mobility which partially counteracts the mobility increase achieved thanks to the strain. This result is very important, since it shows the existence of a lower limit to the T_{Si} that may be used in ultrathin Si/SiGe-OI MOSFETs if we want to keep a high mobility value.

In order to show the existence of this limit, we simulated the electron transport in these strained-Si/SiGe-OI structures by the Monte Carlo method. Electron quantization in the inversion layer was taken into account by self-consistently solving the Poisson and Schrodinger equations. A simple nonparabolic band model was assumed taking $\alpha = 0.5$ eV⁻¹. The effect of strain in the silicon layer is included only in the band structure as the valley splitting energy $\Delta E = 0.67x$ (x being the germanium mole fraction), assuming that the strain does not modify the shape of the

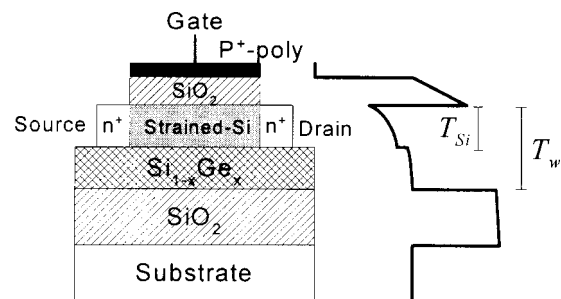


FIG. 1. Simulated strained-Si inversion layer on SiGe-OI substrate. (Si layer thickness T_{Si} , SiGe-layer thickness T_{SiGe} , gate oxide thickness $T_{\text{ox}} = 5$ nm, buried oxide thickness $T_{\text{box}} = 80$ nm.)

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