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Monte Carlo simulation of double-gate silicon-on-insulator inversion layers: The role of volume inversion

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The electron mobility in a double-gate silicon-on-insulator (DGSOI) device is studied as a function of the transverse effective field and silicon layer thickness. The contributions of the main scattering mechanisms (phonon scattering, surface roughness scattering due to both $Si-SiO_2$ interfaces, and Coulomb interaction with the interface traps of both interfaces) are taken into account and carefully analyzed. We demonstrate that the contribution of surface scattering mechanisms is by no means negligible; on the contrary, it plays a very important role which must be taken into account when calculating the mobility in these structures. The electron mobility in DGSOI devices as T_w decreases is compared with the mobility in single-gate silicon-on-insulator structures (i) when only phonon scattering is considered, (ii) when the effect of surface-roughness scattering is taken into account, and (iii) when the contribution of Coulomb interaction with charges trapped at both interfaces is taken into consideration (in addition to phonon and surface roughness scattering). From this comparison we determined (in the three cases above) the existence of the following three regions: (i) A first region for thick silicon layers ($T_w > 20-30$ nm), where mobility for both structures tends to coincide, approaching the bulk value. (ii) As T_w decreases we show that volume inversion modifies the electron transport properties by reducing the effect of all scattering mechanisms. Accordingly, the electron mobility in DGSOI inversion layers increases by an important factor which depends on the silicon thickness and the transverse effective field. (iii) Finally, for very small thicknesses, the limitations to electron transport are due to geometrical effects, and therefore the two mobility curves, which again coincide, fall abruptly. We show the existence of a range of thicknesses of a silicon layer (between 5 and 20 nm in which electron mobility is improved by 25% or more. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1358321]

I. INTRODUCTION

Silicon-on-insulator (SOI) technology is considered for future electronic technology because of the many advantages that these devices present when compared to their bulk counterparts,[1–4] and because of its compatibility with existing fabrication facilities. Thus a lot of effort has been spent in recent years to study carrier transport in these devices.

In this respect, double-gate metal–oxide–semiconductor field-effect-transistors (DGMOSFETs) are currently considered a serious alternative to standard-bulk MOSFETs to increase the integration capacity of silicon technology in the near future. A dual-gate-silicon-on-insulator (DGSOI) structure consists, basically, of a silicon slab sandwiched between two oxide layers. A metal or a polysilicon film contacts each oxide. Each one of these films acts as a gate electrode (front and back gate), which can generate an inversion region near the $Si-SiO_2$ interfaces, if an appropriate bias is applied. Thus we would have two MOSFETs sharing the substrate, source, and drain. The outstanding feature of these structures lies in the concept of volume inversion, introduced by Balestra *et al.*:[5] if the Si film is thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers, and the operation of this device is similar to the operation of two conventional MOSFETs connected in parallel. However, if the Si thickness is reduced, the whole silicon film is depleted and an important interaction appears between the two potential wells. In such conditions the inversion layer is formed not only at the top and bottom of the silicon slab (i.e., near the two silicon–oxide interfaces), but throughout the entire silicon film thickness. It is then said that the device operates in ''volume inversion,'' i.e., carriers are no longer confined at one interface, but distributed throughout the entire silicon volume. Several authors have claimed that volume inversion presents a significant number of advantages, such as (i) enhancement of the number of minority carriers; (ii) increase in carrier mobility and velocity due to reduced influence of scattering associated with oxide and interface charges and surface roughness; (iii) as a consequence of the latter, an increase in drain current and transconductance; (iv) decrease of low-frequency noise, and (v) a great reduction in hot-carrier effects.[5]

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