Properties of Ultra-Thin Wafer-Bonded Silicon-on-Insulator MOSFET's

Baquer Mazhari, Sorin Cristoloveanu, Dimitris E. Ioannou, *Member, IEEE*, and Anthony L. Caviglia, *Member, IEEE*

Abstract—**The characteristics of MOS transistors fabricated in ultra-thin (50–70 nm) wafer-bonded SOI films are reported. Strong interface coupling effects are found to govern the properties of the front and back channels. Simple theoretical models are proposed which explain the substantial variations of the transconductance and subthreshold slope as the opposite interface is scanned from inversion to total depletion and accumulation. These MOSFET's behave very well and demonstrate that high-carrier mobilities and low densities of defects can be obtained at both interfaces even in ultra-thin SOI structures.**

I. Introduction

The advantages of silicon on insulator (SOI) MOSFET's such as radiation hardness and reduced parasitic capacitance are well known. Recently, it has been confirmed that MOSFET's made on fully depleted ultra-thin films have additional benefits of nearly ideal subthreshold slope [1], increased saturation current [2], and reduced short-channel/floating body effects [3]. To date, most of the thin SOI films have been synthesized by oxygen implantation (SIMOX). The purpose of this paper is (1) to demonstrate that high quality ultra-thin films can also be prepared by wafer bonding and (2) to investigate a number of interface coupling effects which become very prominent in ultra-thin SOI-MOSFET's. The influence of the interface coupling on the threshold voltage has already been studied extensively [4]. Very recently, an excellent paper has been published by Wouters *et al.* [5] on the modeling of the subthreshold region. The next section provides a complementary analysis of the subthreshold slope, which can be directly used for interface parameter extraction. An original model of the transconductance, that accounts for the minority carrier spreading in the film, is proposed in Section III. The last section will focus on the discussion of the most specific properties of the very thin Si film and interfaces in wafer-bonded SOI.

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B. Mazhari is with the Department of Electrical Engineering, University of Maryland, College Park, MD 20742.

S. Cristoloveanu is with the Department of Electrical Engineering, University of Maryland, College Park, MD 20742, on leave from LPCS, ENSERG, B.P. 257, 38016, Grenoble Cedex, France.

D. E. Ioannou is with the Department of Electrical and Computer Engineering, George Mason University, Fairfield, VA 22030.

A. Caviglia is with the Allied-Signal Aerospace Technology Center, Columbia, MD 21045.

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SOI films of thickness t_{si} = 50–150 nm were fabricated by the wafer bonding and etch-back technique described recently [6]. n-channel enhancement-mode devices were processed with a standard CMOS technology in these SOI substrates, where the residual doping was p-type ($N_A \simeq 2 \times 10^{16}$ cm^{-3}) and the thicknesses of the front and back gate oxides were t_{ox1} = 27 nm and t_{ox2} = 850 nm, respectively.

II. Subthreshold Characteristics

The front channel characteristics were measured for various back gate voltages. It is seen from Fig. 1(a) that with the back interface in depletion, an excellent swing is obtained (69 mV/decade). This demonstrates the high quality of *the front and back* Si-SiO_2 interfaces, as they both affect the subthreshold characteristics in the present case. Fig. 1(b) shows the back channel characteristics where again the maximum slope is found with the opposite (front) interface kept in depletion.

The current can flow either at the front interface, back interface or throughout the film [7]. Since the front and back gate voltages (V_{G_1}, V_{G_2}) can be used independently to control the current, a generalized subthreshold swing S_{ij} is defined

$$S_{ij} = \left(\frac{d \log_{10} I_{D_j}}{dV_{G_i}}\right)^{-1} \simeq 2.3 \frac{kT}{q} \frac{dV_{G_i}}{d\phi_j} \quad (1)$$

where the subscripts, i, j take the values 1 or 2, corresponding to the front or back interfaces; the subscript i shows the gate that is operated, while j indicates the interface where most of the current is driven. We assume a *linear* variation of the potential across the *depleted thin* film (i.e., a constant vertical field: $E_{si} \simeq (\phi_f - \phi_b)/t_{si}$). The variations $\Delta\phi_{1,2}$ of the interface potentials with $\Delta V_{G1,2}$ are determined by taking the derivatives of the Gauss law relationships at the front and back interfaces

$$C_{ox1,2}(\Delta V_{G1,2} - \Delta\phi_{1,2}) = C_{it1,2}\Delta\phi_{1,2} + C_D(\Delta\phi_{1,2} - \Delta\phi_{2,1}) \quad (2)$$

where $C_D = \epsilon_s/t_{si}$ is the capacitance of the depleted Si film and $C_{it1,2} = qN_{it1,2}$ are the capacitances due to front and back interface state densities $N_{it1,2}$. As usual, we ne-

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