SILICON-ON-INSULATOR "GATE-ALL-AROUND DEVICE"

J.P. Colinge, M.H. Gao, A. Romano-Rodríguez, H. Maes, and C. Claeys

IMEC, Kapeldreef 75, 3030 Leuven, Belgium

Abstract

This paper describes the process fabrication and the electrical characteristics of an SOI MOSFET with gate oxide and a gate electrode not only on top of the active silicon film, but also underneath it. Device fabrication is simple and necessitates only a single additional mask and etch step, compared to standard SOI processing. The device shows evidence of volume inversion (inversion is observed not only in surface channels, but through the entire thickness of the silicon film). Because of the presence of two channels and because of reduced carrier scattering within the bulk of the silicon film, the transconductance of the "Gate-All-around" device is more than twice that of a conventional SOI device, and its subthreshold slope is nearly 60 mV/decade at room temperature.

Introduction

Different theoretical studies have shown that thin-film Silicon-On-Insulator (SOI) devices with a gate electrode both above and below the active silicon film would allow one to obtain extremely interesting electrical properties such as high transconductance and reduced short-channel effects. Figure 1 presents the schematic cross-section of a conventional SOI device and that of a device with top and bottom gate electrode. In the conventional MOSFET, the active silicon film sits on top of a 400 nm-thick buried oxide layer (SIMOX material), and the underlying silicon substrate can be used as a back gate. In the proposed "Gate-All-Around" structure, the active silicon sits on a thin, gate-quality oxide and on a polysilicon gate electrode. Because of the extremely good control of the charges within the active silicon when top and bottom (T&B) gate is provided, significant short-channel threshold rolloff has been predicted in devices with T&B gate [1]. In addition, it has been found theoretically that the thin silicon film in which T&B gate devices are made can become completely inverted when a gate voltage is applied (*i.e.*: inversion is not confined within top and bottom inversion channels, but the entire film becomes inverted at all depth x in the silicon film [2]) (Figure 2). This particularity provides the device with enhanced transconductance performances, since inversion within the volume of the silicon presents less scattering than surface inversion. A third advantage of this type of device is its potentially high total-dose hardness. Indeed, the threshold shift induced in a MOSFET by exposure to dose irradiation is proportional to the square of the thickness of the oxide in contact with the active silicon [3]. In conventional SOI MOSFETs, the buried oxide underneath the device has a thickness of 400 nm, typically. Charges are created in this relatively thick oxide by dose exposure and cause important threshold shifts in thin-film devices [4]. In the T&B gate device proposed here, the active part of the device is only in contact with thin, gate-quality oxide, which should minimize radiation-induced threshold voltage shifts.

Device Fabrication

The devices were fabricated using a simple 3 µm process and commercial 125 mm SIMOX substrates. The original thickness of the silicon film is 180 nm. A thin pad oxide is grown, and silicon nitride is deposited. Using a mask step, the nitride and the silicon are etched to define the active areas. An oxidation step (200 nm oxide) is used to round the edges of the silicon islands, after which the nitride and the pad oxide are stripped. A mask step is then used to cover the entire wafer with resist except areas which correspond to an oversize of the intersection between the active area and the poly gate layers. The wafers are then immersed in buffered HF. At this step the oxide on the sidewalls of the silicon islands as well as the buried oxide are etched, and a cavity is created underneath the center part of the silicon islands (Figure 3). The wafers are removed from BHF once the cavity etch is completed. At this point, the device looks like a silicon bridge supported by its extremities (which will later on become source and drain), which is hanging over an empty cavity. Gate oxidation is then carried out. In this step, a 50 nm-thick gate oxide is grown over all the exposed silicon (top, bottom and edges of the active silicon, as well as on the silicon substrate in the bottom of the cavity). Boron is implanted to adjust the threshold voltage, and polysilicon gate material is then deposited and doped n-type. Because of the extremely good conformality of LPCVD polysilicon, the gate oxide over the cavity is completely coated with polysilicon, and a gate is formed on the top, the sides and the bottom of the channel area (hence the name of gate-all-around (GAA) device). The polysilicon gate is then patterned using conventional lithography and anisotropic plasma etch. Source and drain are formed using phosphorous implantation followed by an annealing step. CVD oxide is deposited, and contact holes are opened. An aluminum metallization step completes the process. Figure 4 presents a bird's eye view of the device after source and drain formation, Figure 5 show a top view of the device, and Figure 6 show a TEM cross-section of the channel area, perpendicular to the current flow [5]. The difference in grain size in the polysilicon gate layers above and below the device is due to the fact that the polysilicon is doped by heavy phosphorous ion implantation. The upper part of the polysilicon is amorphized during this process, and it recrystallizes into large grains during the subsequent dopant redistribution annealing step (800ºC, 8 hours), while the unamorphized bottom polysilicon retains its original as-deposited columnar texture. It is worthwhile mentioning that

CH2865-4/90/0000-0595 $1.00 © 1990 IEEE