"Linear Kink Effect" Induced by Electron Valence Band Tunneling in Ultrathin Gate Oxide Bulk and SOI MOSFETs

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***Abstract*—In this paper, evidence will be provided for the existence of a new class of floating body effects, occurring in SOI and bulk MOSFETs in the linear operation regime and called here the linear kink effects (LKEs). It will be shown that for a sufficiently large front-gate voltage V_G, the transconductance g_m exhibits a second peak, both for n- and p-channel devices. The effect is most pronounced for partially depleted (PD) n-MOSFETs or bulk MOSFETs at cryogenic temperatures. It occurs as well in fully depleted (FD) transistors, with the back-gate preferably biased into accumulation. Associated with the LKE in the drain current, there is a strong increase of the low-frequency noise spectral density S_I. Similar as for the impact-ionization related noise overshoot, it is observed that the nature of the spectrum changes from $1/f$-like to Lorentzian in the LKE region. It is finally shown that the switching off transients change their sign from negative to positive for $V_{G\,\mathrm{on}}$ above the LKE threshold, giving evidence for the presence of majority carriers in the film during the ON phase.**

***Index Terms*—Floating body effects, generation lifetime, kink effect, Lorentzian noise spectrum, noise overshoot, switch off transient, transconductance peak.**

I. INTRODUCTION

An excess of the drain current, related to the floating body effect and hole generation by impact ionization can appear in the saturation region of SOI MOSFETs [1]. This mechanism has been reported for drain voltages below the band-gap voltage ($V_D = 0.7$ V) by including additional energy gain mechanisms to overcome the thresholds of impact-ionization processes [2], [3]. In this paper we examine a new type of "kink effect" already appearing in the linear regime ($|V_D| < 100$ mV) of ultrathin gate bulk and SOI MOSFETs: the linear kink effect (LKE). As will be shown, the LKE gives rise to a second peak in the linear transconductance g_m and an overshoot in the low-frequency noise spectral density S_I for front-gate voltages exceeding about 1.1 V in absolute value. The effect occurs both in partially (PD) and fully depleted (FD) devices. For the latter case, the back gate should preferably be biased in accumulation. It is also observed that the second g_m peak is relatively less pronounced for short device lengths L and is suppressed when there is a large subthreshold leakage current. Moreover, the LKE affects the switching off behavior of the transistors drastically, which has consequences both for circuit operation and generation lifetime extraction. Finally, a simple model will be proposed, explaining the observations in terms of electron valence band tunneling through the ultrathin gate oxide.

II. DEVICES TECHNOLOGY

The LKE is experimentally investigated at low drain bias V_D for SOI MOSFETs fabricated in a 0.1-μm SOI process using a PELOX isolation scheme, a 2.5-nm nitrided gate oxide (NO), a 150-nm polysilicon gate, and 80-nm nitride spacers [4]. Processing was performed on 200-mm diameter UNIBOND (U) wafers, resulting in a final film thickness of 100 nm (PD) or 30 nm (FD). The buried oxide thickness was 400 (PD) and 200 nm (FD), respectively. The test structures have a common gate/common source configuration with separate drain pads. As there is no film contact for these SOI MOSFETs, complementary investigations have also been performed on devices fabricated in a 0.13-μm bulk CMOS process. These CMOS devices are using an STI isolation scheme, 2 nm reoxidized nitrided gate oxide (RNO), 150-nm polysilicon gate, and 80-nm nitride spacers. The transistor width is $W = 10$ μm, while channel lengths ranging from 0.1 up to 10 μm have been studied. By combining results obtained under different controlled experimental conditions, the LKE is experimentally analyzed.

III. LKE: EXPERIMENTS AND ANALYSIS

The LKE is clearly identified by an excess of the drain current and a "second peak" in the transconductance for usual experimental conditions at room temperature in PD SOI MOSFETs [Fig. 1(a)] or FD SOI MOSFETs with the appropriate back gate bias (V_{BG}) [Fig. 1(b)]. From Fig. 1(b), it is obvious that a similar effect occurs for FD n-MOSFETs, when the back-gate becomes (more) accumulated, i.e., for a more negative V_{BG}. Comparing the PD and FD transistors of Fig. 1(a) and (b), respectively, it is observed that the second g_m peak occurs at the same front-gate voltage. The largest Δg_m is found for the FD device at $V_{\mathrm{BG}} = -20$ V. For the n-channel devices studied, the second peak typically occurs for a V_G around 1.1 V.

The result for the p-channel PD MOSFET counterparts is shown in Fig. 2. Note in Fig. 2 also the presence of a hysteresis effect: while there is a pronounced second g_m peak for the accumulation to inversion gate voltage sweep, a much smaller kink

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