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REVIEW PAPER

THE LOW-FREQUENCY NOISE BEHAVIOUR OF SILICON-ON-INSULATOR TECHNOLOGIES

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Abstract—In this overview, the low-frequency noise behaviour of devices fabricated in silicon-on-insulator technologies is described. The different potential noise sources are analysed and illustrated by experimental results, mainly obtained on MOSFETs. Some SOI-specific noise behaviour is highlighted, as for instance the kink-related excess low-frequency noise overshoot. It is shown furthermore that SOI MOSFETs suffer from so-called random telegraph signals, which can originate from the front- or the back-gate dielectric, or from defects located in the thin Si active layer. The impact of the substrate type (SIMOX, bonded, ZMR, ...) is discussed. At the same time, it is shown that the used technology and device structure can have a pronounced effect on the LF noise performance. Finally, the response of SOI MOSFETs on ionizing radiation (γs, X-rays, ...) is studied through the LF noise degradation, in view of radiation-hardened applications. Copyright © 1996 Elsevier Science Ltd

1. INTRODUCTION

Since the early days of semiconductor electronics, low-frequency (LF) noise has attracted considerable interest (for recent overviews see e.g. Refs [1,2]). The research effort has been driven by two major factors. On the one hand, LF noise is of crucial importance for analog applications (amplifiers, read-out electronics, solid-state detectors, ...), whereby the goal is to minimize the system noise, either by a proper choice of technology, or by optimum design. For that purpose, however, a thorough understanding of the basic noise mechanisms is required. While the physics of generation-recombination (GR) noise is well-established (see e.g. Refs [3 and 4]), the theoretical basis of so-called flicker noise, characterized by a $1/f$-like spectral intensity, is still a matter of long-lasting debate. In the McWhortger model[5], the $1/f$ noise (f the frequency) is primarily generated by fluctuations in the number of carriers and is therefore also called the Δn model. The Hooge theory, on the other hand, assumes that fluctuations in mobility, through the stochastic nature of carrier scattering events, cause the LF noise[6]. Irrespective of the exact origin, numerous studies have demonstrated the usefulness of LF noise as a tool for technological evaluation[7], whereby it is often observed that the noise is much more sensitive to the presence of flaws or defects, existing along the path of current flow. In parallel, continuous attempts have been undertaken to use LF noise as a non-destructive lifetime evaluation tool, for instance for components which will be submitted to ionizing radiation[8].

Silicon-on-sapphire (SOS) and more recently silicon-on-insulator (SOI) devices were originally developed for rad-hard applications[9], whereby dependent on the tolerance level, one can distinguish space components on the one hand, or on the other hand, for high cumulated doses (in the Mrad(Si) range), nuclear and military instrumentation. One particular class of satellite circuits are the so-called read-out electronics for focal-plane arrays, which generally operate at cryogenic temperatures (77 K or 4.2 K). As recently reviewed, SOI technologies offer excellent perspectives in this field[10]. While CMOS on bulk Si substrates dominates the largest part of the IC market, it is known for quite some time that SOI offers some specific advantages[11]. It is even expected that for deep-submicron technologies, SOI CMOS may outperform standard bulk[12], which is important for future low-power, low-voltage applications[13]. In fact, the feasibility of a 0.1 μm CMOS technology on SOI has been demonstrated recently, showing excellent delays of 20 ps[13]. This growing interest in SOI is considerably stimulated by the improvement in the substrate quality, the reduction in cost and the growing number of suppliers[9,14], whereby SIMOX (separation by ion implantation) and BESOI (bond and etchback SOI) are the main contenders to date.

From a fundamental LF noise viewpoint, SOI components form an interesting challenge, as indicated schematically in Fig. 1 for a MOSFET. Indeed, besides the "natural" noise sources which are situated at the front Si–SiO$_2$ boundary, other sources can also come into play, depending on the nature of the device