$$S = kT\ln(10)\left(1 + \frac{C_D + C_{IT}}{C_{OX}}\right)$$

where C_D is the capacitance of the depletion region, C_{OX} is the oxide capacitance, and C_{IT} is the capacitance due to the interface states ($C_{IT} = qD_{IT}$, where D_{IT} is the interface state density per eV per cm²). D_{IT} is estimated from the subthreshold slope to be $\sim 10^{12}cm^{-2}eV^{-1}$, which agrees well with values determined from C-V and gate-controlled-diode measurements on similar wafers [3].

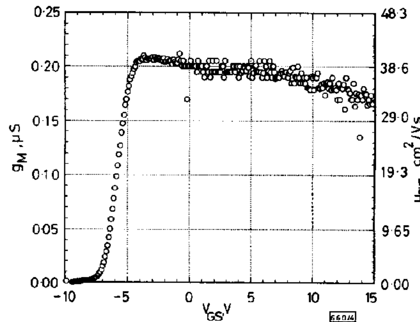

Fig. 4 *Room temperature transconductance g_m and field-effect mobility μ_{FE} for SiC self-aligned MOSFET with gate length 20µm, channel width 60µm, and oxide thickness 80nm*

Fig. 4 shows transconductance g_m and field-effect mobility μ_{FE} at a drain-to-source voltage of 40mV for a MOSFET with a gate length of 20µm and a channel width of 60µm. The peak mobility is 40cm²/Vs, which is comparable to values obtained on non-self-aligned 6H-SiC devices.

In conclusion, we report a self-aligned polysilicon gate MOSFET in 6H-SiC with low source-drain resistance and improved drive current. The peak channel mobility is 40cm²/Vs at room temperature and the subthreshold slope is 500mV/decade. These results indicate that self-aligned MOSFETs can be fabricated in 6H-SiC with a low source-drain resistance.

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Silicon on insulator material technology

M. Bruel

Indexing terms: Silicon-on-insulator, Wafer bonding

A silicon on insulator material technology based on wafer bonding is described, in which a heat treatment induces an in-depth microslicing of one of the two bonded wafers previously implanted with hydrogen. The basic phenomena, and the first physical and electrical characterisations are discussed briefly.

Introduction: For the past few years there has been a growing interest in SOI material technology [1, 2] based on wafer bonding and etch-back (BESOI). To achieve thin uniform SOI layers, the BESOI technology involves either a etch stop layer or the combination of accurate thickness mapping and fine local thinning with a localised plasma.

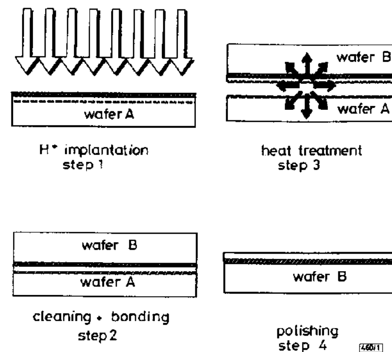

Fig. 1 *Principle of Smart-Cut process*

The new process described in this Letter was developed at LETI under the code name 'IMPROVE' and is referred to as 'Smart-Cut'. It essentially comprises four steps (Fig. 1):

Step 1: Ion implantion (dose = $2 \times 10^{16} - 1 \times 10^{17} cm^{-2}$) of hydrogen ions in a silicon wafer A: This wafer is preferably capped before implantation with a dielectric layer, e.g. thermally grown SiO_2. This dielectric layer becomes the buried oxide of the SOI structure.

Step 2: Hydrophilic bonding at room temperature of wafer A to a wafer B: Wafer B is either bare or capped. Both wafers are previously cleaned using a modified RCA process. Wafer B plays a key role in the Smart-Cut process as a stiffener and provides the bulk silicon under the buried oxide in the SOI structure.

Step 3: Two-phase heat treatment of the two bonded wafers: During the first phase (400 – 600°C), the implanted wafer A splits into two parts: a thin layer of monocrystalline silicon remaining bonded to wafer B and the rest of wafer A, which can be recycled for use as another wafer B. The second high temperature treatment phase (>1000°C) aims to strengthen the chemical bonds.

Step 4: Fine polishing: After splitting, the layer exhibits a microroughness (Fig. 2) which makes chemomechanical polishing of the surface necessary.