Bonding of silicon wafers for silicon-on-insulator

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Several aspects of a new silicon-on-insulator technique utilizing bonding of oxidized silicon wafers were investigated. The bonding was achieved by heating in an inert atmosphere a pair of wafers with hydrophilic surfaces contacted face-to-face. A quantitative method for the evaluation of the surface energy of the bond based on crack propagation theory was developed. The bond strength was found to increase with the bonding temperature from about 60–85 $\mathrm{erg/cm^2}$ at room temperature to $\simeq 2200\ \mathrm{erg/cm^2}$ at 1400 °C. The strength was essentially independent of the bond time. Bonds created during 10-s annealing at 800 °C were mechanically strong enough to withstand the mechanical and/or chemical thinning of the top wafer to the desired thickness and subsequent device processing. A model was proposed to explain three distinct phases of bonding in the temperature domain. Electrical properties of the bond were tested using metal-oxide-semiconductor (MOS) capacitors. The results were consistent with a negative charge density at the bond interface of approximately $10^{11}\ \mathrm{cm^{-2}}$. A double-etch-back procedure was used to thin the device wafer to the desired thickness with ± 20 nm thickness uniformity across a 4-in. wafer. The density of threading dislocations in the remaining silicon layer was 10^2–$10^3\ \mathrm{cm^{-2}}$, and the residual dopant concentration less than $5\times 10^{15}\ \mathrm{cm^{-3}}$, both remnants of the etchstop layer. Complimentary metal-oxide-semiconductor (CMOS) devices made in the 20–100 nm silicon thick layers had subthreshold slopes of 68 mV/decade (both *n*- and *p*-channel MOS transistors). The effective carrier lifetime was 15–20 μs in 80- and 300-nm-thick Si films and the interface state density at the Si film-buried oxide interface was $\leqslant 5\times 10^{10}\ \mathrm{cm^{-2}}$.

INTRODUCTION

There are three popular approaches to creating a generic (nonmask-specific) silicon-on-insulator (SOI) wafer. The oldest, silicon-on-sapphire (SOS), has been investigated for more than 20 years. Despite numerous improvements, the quality of the silicon layer is still far inferior to bulk silicon. A high density of extended defects (microtwins in particular), contamination with aluminum from the substrate, its high cost, and the lack of a substrate biasing capability limit its potential applications. Two more recent SOI contenders, zone melt recrystallization (ZMR) and separation by implanted oxygen (SIMOX), also exhibit certain drawbacks. ZMR suffers from silicon voids, protrusions, threading dislocations ($\sim 10^6\ \mathrm{cm^{-2}}$), wafer warpage, and surface roughness and waviness. The buried oxide in SIMOX has poor quality interfaces with silicon, Si inclusions, and limited thickness flexibility. Its silicon layer in the best experimental material contains ($\leqslant 10^5$) threading dislocations per square centimeter and a significant level of numerous contaminants.

A permanent bond between highly polished surfaces of silicon and glass[1] or between oxidized silicon wafers[2] has been obtained by electric field assisted bonding at high temperatures in an inert atmosphere. Recently, a similar bonding effect obtained without any electric field or externally applied pressure was reported by Lasky[3] and Shimbo *et al.*[4] The bonding process accompanied by subsequent removal of most of one of the wafers by mechanical and/or chemical means creates a generic SOI wafer. The quality of the silicon and $\mathrm{SiO_2}$ layers and the interface between them in such a structure is superior to that of other SOI techniques. This bond-and-etchback silicon-on-insulator (BESOI) technique provides an insulating oxide and a silicon film of high quality (comparable to bulk), as well as thermal oxide interfaces between the buried $\mathrm{SiO_2}$ and the film and substrate silicon. It inherently permits the use of a wide range of thicknesses of both films, which allows for more design flexibility.

BESOI TECHNIQUE

Our version of the BESOI process involves the following steps:

(1) Formation of an etch stop in one of the wafers (which, following Lasky's nomenclature,[3] is referred to as the seed wafer), and oxidation of the wafer;

(2) contacting two oxidized wafers (the seed and the handle[3] wafers) face-to-face with the surfaces conditioned to be hydrophilic at room temperature;

(3) bonding the contacted wafers at elevated temperatures in nitrogen;

(4) etching, or lapping and etching, of the seed wafer with a selective etch.

In the following sections, we will introduce a quantitative method of measurement of the strength of the bond between two wafers and, subsequently, discuss each of the steps of the technique. Evaluation of the structural and electrical parameters of this SOI material and CMOS devices made in it will be given as well.