Wafer bonding for silicon-on-insulator technologies

J. B. Lasky
IBM General Technology Division, Essex Junction, Vermont 05452

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A silicon wafer bonding process is described in which only thermally grown oxide is present between wafer pairs. Bonding occurs after insertion into an oxidizing ambient. It is proposed the wafers are drawn into intimate contact as a result of the gaseous oxygen between them being consumed by oxidation, thus producing a partial vacuum. The proposed bonding mechanism is polymerization of silanol bonds between wafer pairs. Silicon on insulator (SOI) is produced by etching away all but a few microns of one of the bonded pair. Capacitor measurements show a 27 μs minority-carrier lifetime and no degradation of the SOI-insulator interface. In addition, there is negligible charge at the bonding interface making the technique attractive for three-dimensional as well as planar SOI applications.

During the past several years, there has been intensive effort to produce electronic quality silicon on insulator (SOI) for very large scale integration (VLSI) applications. The methods used may be placed in two broad categories. A silicon layer may be formed above an existing oxide layer. Examples are laser or strip heater recrystallization, and selective epitaxial methods.[1] Generally, the quality of the silicon formed is inferior to that associated with bulk silicon processing. The second category is comprised of methods which form an oxide layer beneath an existing high quality silicon layer. Examples are oxidized porous silicon and oxygen ion implantation. Generally, these methods result in an inferior oxide and the quality of the SOI may be degraded during oxide formation. The purpose of this letter is to describe a bonding procedure and its use for forming silicon on insulator. The process results in a thin silicon layer above a thermally grown oxide. Electrical characterization is performed using capacitor structures. The results show that the quality of the silicon layer and the underlying oxide is not degraded from its original "bulk" quality. Aspects of this process, though not the bonding process, are similar to the "polycrystalline silicon handle" dielectric isolation method,[2] and methods which substitute a silicon wafer for the polycrystalline silicon handle.[3]

The silicon-on-insulator process consists of growing a lightly doped epitaxial layer on a heavily doped wafer, growing a thermal oxide, and bonding this wafer to a lightly doped "handle" wafer. The heavily doped wafer is then removed using a selective etch,[4] leaving a thin SOI layer above the thermally grown oxide. The bonding is achieved by pressing the oxidized surfaces of two wafers together and inserting them into an oxidizing atmosphere at greater than 700 °C. Typically, the wafers are pressed together to expel most of the air from between them. However, even if the wafers are just laid one on top of the other, bonding occurs about half the time. Normally, bonding occurs over the entire wafer surface except in 1-cm-diam regions where particles keep the wafers apart. Bonding has been demonstrated with thermally grown oxide thicknesses ranging from native oxide to 520 nm on either or both wafers. In the cases where native oxides are bonded together, bonding in a steam or a dry oxygen ambient has been observed over the temperature range of 700–1050 °C, 1050 °C being the highest temperature investigated. Bonding does not occur if nitride is on one or both wafer surfaces. If the heating is done in nitrogen, only a small fraction of the wafer area is bonded or bonding may not occur at all.

To evaluate the electrical quality of silicon and silicon/oxide interfaces subjected to bonding, two capacitor structures were fabricated. These are illustrated in Fig. 1. The structure in Fig. 1(a) was made by growing a 6-μm epitaxial layer doped to 1×10^{16} with As on a 0.008 Ω cm boron-doped wafer. The boron-doped wafer is referred to as the "seed" wafer and the epitaxial layer will be made into SOI. After growth of 500 nm of thermal oxide this wafer was bonded to a second wafer, which we refer to as the "handle" wafer. The handle wafer, in this case, is an n^- wafer whose surface had previously been degenerately doped by As ion implantation. A selective etch[4] was used to remove the p^+ "seed" substrate, thus forming the SOI layer. The surface of the SOI layer was then doped by As^+ ion implantation, 40 nm of oxide grown, 0.15-cm-diam dots defined, and the silicon surrounding the dots removed by etching in KOH. A 500 nm oxide was grown and the dots contacted with aluminum. Aluminum deposition on the back of the handle wafer and a forming gas anneal completed fabrication. The n^- handle wafer acts as one electrode for the 500 nm "gate" oxide, the SOI layer the other. Thus, the charge at the back surface of the SOI layer and the minority-carrier generation lifetime[5] may be determined by examining the capacitance-voltage (C-V) characteristics. Measurements were made on 138, 0.15-cm-diam capacitors. The flatband voltage for the

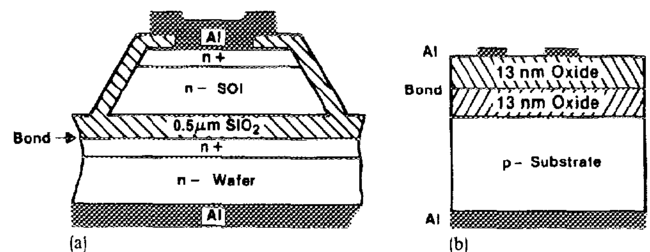

FIG. 1. Capacitor structures used to evaluate (a) SOI quality and (b) charge at bonding seam.

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