

VI. SUMMARY

Quick turn-around line (QTL) technology has been developed to fabricate custom LSI circuits in a short period of time.

The main features of this technology are summarized as follows:

- 1) Electron-beam direct writing for multilevel metallization.
- 2) Automatic data handling and transformation from logic design data to electron-beam writing data.
- 3) Dry process technology including RIBE for Al-Si-Cu etch without 2nd layer metallization process.

Using this technology, a number of 1500-gate ECL gate arrays have been produced for use in main frame computers. Electron-beam irradiation on the device induces a decrease of h_{FE} , which recovers with a 450°C anneal for 15 min in N_2 .

Bias-temperature tests have been done for various logic circuits, and showed no failures with over 1000 h of testing.

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Threshold Voltage of Thin-Film Silicon-on-Insulator (SOI) MOSFET's

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Abstract—The charge coupling between the front and back gates of thin-film silicon-on-insulator (SOI: e.g., recrystallized Si on SiO_2) MOSFET's is analyzed, and closed-form expressions for the threshold voltage under all possible steady-state conditions are derived. The expressions clearly show the dependence of the linear-region channel conductance on the back-gate bias and on the device parameters, including those of the back silicon-insulator interface. The analysis is supported by current-voltage measurements of laser-recrystallized SOI MOSFET's. The results suggest how the back-gate bias may be used to optimize the performance of the SOI MOSFET in particular applications.

I. INTRODUCTION

THE RECENTLY demonstrated [1], [2] dramatic improvement in the quality of polycrystalline-silicon (poly-silicon) films yielded by zone-melting recrystallization has spurred new interest in silicon-on-insulator (SOI) integrated circuits and devices. This new technology provides an alterna-

tive to silicon-on-sapphire (SOS) in the fabrication of monolithic circuits comprising advantageous dielectrically isolated devices [3]. The silicon-on-oxide (hereinafter termed SOI) technology furthermore has the flexibility to possibly enable the fabrication of radiation-hardened nonplanar ("three-dimensional") integrated circuits [4].

Because SOI films are thin, the electrical properties of MOSFET's fabricated in them are typically influenced by the charge coupling between the front and back gates. For example, the (front-gate) threshold voltage V_{Tf} differs considerably from that of the bulk counterpart and depends on the bias and properties of the back gate. Although much emphasis has been placed on the recrystallization technology, little work has been done on the characterization of the electrical properties of SOI MOSFET's.

Worley [5] derived an analytic model for V_{Tf} of the SOS transistor in which similar charge coupling occurs. However his model, which is unnecessarily complex, pertains only to the usual SOS case in which the back silicon surface is depleted. Sano *et al.* [6] developed a rigorous numerical model for V_{Tf} of the SOI MOSFET that illustrated important parametric dependences. However because no analytic expressions were derived, their illustrations were limited and provided

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