Double-Gate Silicon-on-Insulator Transistor with Volume Inversion: A New Device with Greatly Enhanced Performance

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Abstract—**The double-gate control of silicon-on-insulator (SOI) transistors is used to force the whole silicon film (interface layers and volume) in strong inversion. This original method of transistor operation offers excellent device performance, in particular great increases in subthreshold slope, transconductance, and drain current. A simulation program and experiments on SIMOX structures are used to study the new device.**

I. Introduction

Silicon-on-insulator (SOI) materials are now intensively studied because of their ability to overcome several inherent limitations of bulk silicon VLSI technology (lateral isolation, radiation tolerance, lower parasitic capacitance and power, higher speed, reduced short-channel effects [1], etc). SOI substrates are mainly formed by oxygen implantation (SIMOX), selective oxidation of porous silicon (FIPOS), or overgrowth and recrystallization techniques. A less exploited but very exciting opportunity is to make use of the special multi-interface configuration of SOI substrates for *new* devices to be conceived. In this letter we present experimental and calculated characteristics for a new transistor operated following the concept of *volume inversion,* proposed earlier by our group [2]. The simulation is achieved using a "homemade" computer program which gives the solution of the Poisson equation in multilayer structures [3].

II. Simulation

The physical principle of the device is shown in Fig. 1. A thin Si film is sandwiched between the gate oxide and a thicker buried oxide. Surface inversion channels can be activated either at the top interface, biasing the normal gate V_{G_1}, or at the back interface using the bulk Si substrate as a secondary gate V_{G_2}. We choose to simultaneously bias both gates ($V_{G_2} = KV_{G_1}$), where the coefficient K accounts for the differences in thickness and threshold voltage ($V_{T_1} < V_{T_2}$) between gate oxide and buried oxide (K # 10).

If the film is thicker than the maximum depletion regions induced by the two gates, the inversion channels grow independently, while the middle of the film remains undepleted and dominated by majority carriers. For example, in Fig. 1(a), the film is slightly depleted for $V_{G_1} = 2$ V and only a low

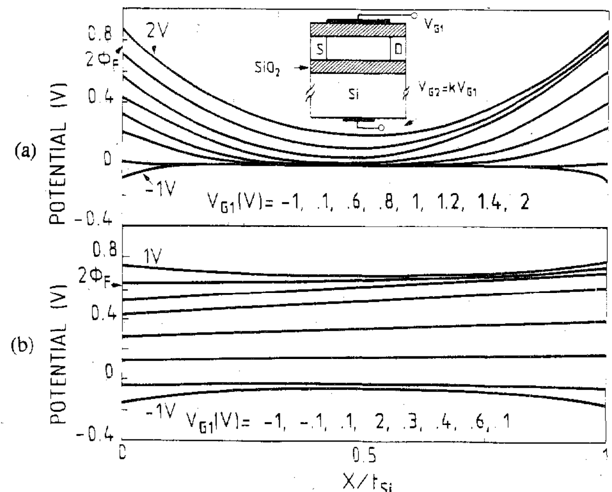

Fig. 1. Potential profiles inside the silicon film for (a) uncoupled (doping $N_A = 4 \times 10^{16}$ cm^{-3}, film thickness $t_{Si} = 300$ nm) and (b) coupled ($N_A = 3 \times 10^{15}$ cm^{-3}, $t_{Si} = 100$ nm) interfaces (27- and 380-nm-thick oxides). X is the distance from the front interface.

coupling appears between the two conducting channels. In this case, the device operation is simply given by the parallel combination of two MOS transistors, i.e., in the linear region

$$I = (WV_D/L)[\mu_1 C_{ox1}(V_{G_1} - V_{T_1}) + \mu_2 C_{ox2}(KV_{G_1} - V_{T_2})]. \quad (1)$$

A different behavior (Fig. 1(b)), caused by the interaction of the two interfaces, occurs in films with normal thickness (< 0.2 μm) and low doping (a few 10^{15} cm^{-3}). For $V_{G_1} = -1$ V, the whole silicon film is in accumulation. For higher V_{G_1}, the electrostatic potential increases at the interfaces and in the film volume, from depletion to weak inversion. Finally, for $V_{G_1} >$ 0.6 V, the potential shift exceeds $2\Phi_F$ in every regions and *all* the film is in strong inversion. We propose to call this new device the "volume-inversion MOS transistor" (VI-MOSFET). The fact that the current drive of VI-MOSFET's is governed by minority carriers, which now are no more confined at an interface, presents tremendous advantages:

a) greatly increased number of minority carriers allowing higher current;
b) reduced influence of surface-induced scattering events and interface defects (fixed charges, slow and fast states);

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