

Scaling the Si MOSFET: From Bulk to SOI to Bulk

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Abstract—Scaling the Si MOSFET is revisited. Requirements on subthreshold leakage control force conventional scaling to use high doping as the device dimension penetrates into the deep-submicrometer regime, leading to undesirable large junction capacitance and degraded mobility. By studying the scaling of fully depleted SOI devices, we note the important concept of controlling horizontal leakage through vertical structures. Several structural variations of conventional SOI structures are discussed in terms of a natural length scale to guide the design. The concept of *Vertical Doping Engineering* can also be realized in bulk Si to obtain good subthreshold characteristics without large junction capacitance or heavy channel doping.

I. INTRODUCTION

OVER THE past thirty years, the primary challenge of VLSI has been the integration of an ever increasing number of devices with high yield and reliability. However, as device dimensions penetrate into the deep-submicrometer regime, the characteristics of a conventional MOSFET approach that of a resistor [1]. This difficulty is traditionally solved by increasing the threshold voltage through increased channel doping. At the same time, reliability constraints have led to reductions in the power supply voltage. The combination of high channel doping and capacitance, increased threshold voltage, and reduced supply voltage, imposes severe tradeoffs between stand-by power and circuit speed.

Brews' empirical scaling rule [2] has provided a successful guideline for the design of the conventional MOSFET. We begin by outlining the implications of the rule in the deep-submicrometer regime, and show how fully depleted SOI (silicon-on-insulator) structures attempt to circumvent the limitations faced by conventional deep-submicrometer devices. We then show that the innovative, but realistic device structures in bulk Si can mimic the SOI philosophy, providing well-behaved devices in the deep-submicrometer regime. Throughout the paper emphasis is placed on the fundamental concepts that govern the operation of such devices. To this end, we provide an analytic framework [3], within which scaling may be naturally understood, supporting the analytic treatment with two-dimensional (2D) numerical simulations [4], [5]¹

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¹Monte Carlo simulations are required to predict the device performance in the turn-on regime [5].

where appropriate. What emerges from our analysis is a natural length scale, which may be used to predict the performance of a class of device structures both in bulk Si and SOI. We conclude by describing a particular device structure which may realize the promise of a well-behaved, deep-submicrometer device operating at room temperature.

II. DIRECT SCALING

Various device scaling rules have been proposed [2], [6], [7]. Brews' empirical rule [2] provides a general guideline for the subthreshold region, and is considered the basic guideline for applications such as dynamic and static memory circuits, where leakage currents in the off state of the devices are important. The intrinsic device parameters for an NMOSFET are L_{eff} , t_{ox} , t_j , and V_{DD} (Fig. 1). (The symbols are defined in Table I.) According to Brews' formula, the effective channel length L_{eff} must be larger than L_{min} in order to achieve good subthreshold behavior

$$L_{\text{min}} = A[t_j t_{\text{ox}}(w_s + w_d)^2]^{1/3} \quad (1)$$

where $A = 0.41 \text{ \AA}^{-1/3}$. Assuming that the device structure (defined by L_{eff} , t_{ox} , t_j , and V_{DD}) is fixed by technology and circuit requirements, and the designer is free only to vary the channel doping N_A , (1) can be reformulated in the following way to relate the channel doping to the intrinsic device parameters:

$$N_A \geq 1.8 \times 10^{17} \text{ cm}^{-3} \frac{[\sqrt{V_{bi}} + \sqrt{V_{bi} + V_{DD}}]^2}{\text{volts}} \cdot \frac{t_j}{500 \text{ \AA}} \cdot \left[\frac{0.1 \text{ \mu m}}{L_{\text{eff}}} \cdot \frac{t_{\text{ox}}}{40 \text{ \AA}} \right]^3 \quad (2)$$

This implies, for example, that in a structure of 0.1- μm channel length, 40- \AA gate oxide, 500- \AA junction depth, and 1.0-V power supply voltage, the channel doping has to be $\geq 10^{18} \text{ cm}^{-3}$.

The effects of the channel doping on the subthreshold behavior of 0.1- μm devices is illustrated in Fig. 2. For the specified device structure ($t_{\text{ox}} = 40 \text{ \AA}$, $t_j = 550 \text{ \AA}$, $L_{\text{eff}} = 0.1 \text{ \mu m}$, and $V_{DD} = 1.5 \text{ V}$), an N_A of 10^{17} cm^{-3} is not sufficient to suppress short-channel effects, and 10^{18} cm^{-3} dopants are necessary. However, high doping leads to high capacitance in Region (I) of Fig. 1, severely limiting the circuit speed. The surface mobility (in Region (II) of Fig. 1) would also be degraded due to the large vertical fields induced by high doping [5], [8]. Both prob-