FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm

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***Abstract*—MOSFETs with gate length down to 17 nm are reported. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET, is proposed. By using boron-doped $Si_{0.4}Ge_{0.6}$ as a gate material, the desired threshold voltage was achieved for the ultrathin body device. The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.**

***Index Terms*—Fully depleted SOI, MOSFET, poly SiGe, short-channel effect.**

I. Introduction

To DEVELOP sub-50-nm MOSFETs, the double-gate structure has been widely studied. This is because for conventional bulk MOSFETs, the high concentration punch-through stopper ($>10^{18}$ cm^{-3}) is indispensable but results in severe drivability and leakage degradation. For the double-gate SOI-MOSFETs, the gates control the energy barrier between the source and drain effectively. Therefore, the short channel effects can be suppressed without increasing the channel impurity concentration [1]–[5].

However, former studies found that the ultrathin body devices have peculiar problems, such as parasitic resistance or threshold voltage controllability [6]–[8]. Furthermore, the complexity of the fabrication process has been a severe problem of double-gate structures. This is because the Si-planar technology is not suitable to form the gate-channel-gate stacked structure that the double-gate device demands. New ideas are sorely needed.

In view of the above problems, we recently proposed a new self-aligned double-gate MOSFET structure. Based on the DELTA structure [10], after reduction of the vertical feature height, the gate-channel-gate stacked structure is realized by a quasi planar technology. In this paper, the fabrication process and the device characteristics in the sub-50 nm gate-length region are presented. We demonstrate the feasibility of the new device structure named FinFET.

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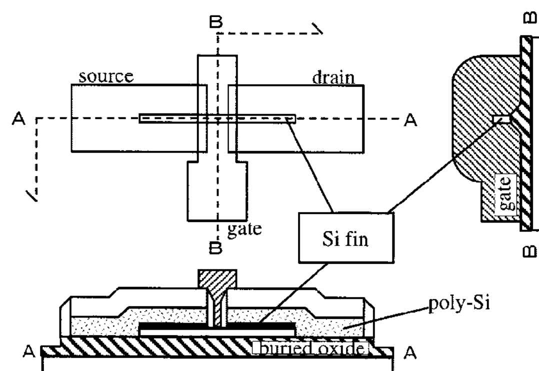

Fig. 1. FinFET typical layout and schematic cross sectional structures.

II. Device Fabrication

The device structure of the FinFET is shown in Fig. 1. As DELTA, the channel was formed on the side "vertical" surface of the Si-fin, and the current flows in parallel to the wafer surface. The device used the elevated S/D process first applied on DELTA [11]. The heart of the FinFET is a thin (~10 nm) Si fin, which serves as body of the MOSFET. A heavily-doped poly-Si film wraps around the fin and makes electrical contact to the vertical faces of the fin. The poly-Si film greatly reduces the S/D series resistance and provide a convenient means for local interconnect and making connections to the metal. A gap is etched through the poly-Si film to separate the source and drain. The width of this gap, further reduced by the dielectric spacers determines the gate length. The channel width is basically twice the fin height (plus the fin width). The conducting channel is wrapped around the surface of the fin. Hence the name—FinFET. Because the S/D and gate are much thicker (taller) than the fin, the device structure is quasiplanar.

Fig. 2 shows the process flow and Fig. 3 shows the SEM pictures at two fabrication step 2 and step 4. The starting material is a SOI wafer with a 400-nm thick buried oxide layer and 50-nm thick silicon film. The measured standard deviation of the silicon film thickness is around 20 A. Although the silicon film thickness determines the channel width, the variation is acceptable for the device uniformity. The variation in the gate length will be a larger source of process variation.

The CVD Si_3N_4 and SiO_2 stack layer is deposited on the silicon film to make a hard mask or cover layer. The cover layer will protect the Si-fin through the fabrication process steps. The fine Si-fin is patterned by electron beam (EB) lithography with 100 keV acceleration energy. The resist pattern is slightly ashed at 5 W and 30 sec to reduce the Si-fin width. Then, using top

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