Point-Contact Pseudo-MOSFET for *In-Situ* Characterization of As-Grown Silicon-on-Insulator Wafers

Sorin Cristoloveanu and Stephen Williams

Abstract—**A pseudo-MOS transistor can be activated in as-grown silicon-on-insulator (SOI) structures without any device processing by using point-contact probes. The measurement setup for *in-situ* operation and typical transistor characteristics are presented. Parameters are extracted which relate to minority and majority carriers, buried oxide, and Si-SiO$_2$ interface.**

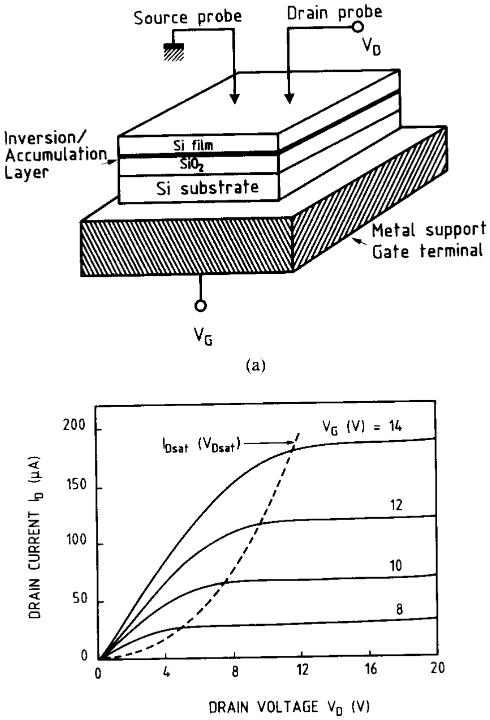
I. Introduction

Silicon on insulator (SOI) and in particular SIMOX are already successful technologies but their quick characterization is a prerequisite for their further optimization and rapid use in microelectronics. The quality of the crystalline silicon film, buried oxide, and interfaces should be known before circuit fabrication in order to avoid costly processing of unsuitable wafers. Of particular importance are the electrical parameters since they are directly related to the performance of integrated circuits. However, nondestructive methods of analysis have, in the past, concentrated on optical techniques while electrical parameters have been evaluated using integrated MOS test structures.

This letter describes a simple electrical technique which takes advantage of the specific configuration of SOI structures and has the potential of being nondestructive. It also allows a more rapid correlation between electrical and synthesis parameters than full processing of MOS test devices.

II. Method

The MOS structure inherent in all SOI materials is used with the bulk Si substrate as a gate terminal, buried oxide as the insulator, and thin Si overlay as the transistor body. To operate *in situ* (without lithography/metallization) this pseudo-MOS transistor (Ψ-MOSFET), low-pressure probes are placed on the upper Si film forming source and drain point contacts (Fig. 1(a)). Biasing the substrate induces a conduction channel at the Si film-SiO$_2$ interface and this allows a full range of $I_D(V_D, V_G)$ curves to be produced. From these characteristics the properties of the buried interface, which represent the most sensitive monitors of SIMOX [1], can be extrapolated. A key point is that both accumulation and inversion channels are probed simultaneously on the same wafer, giving insights into the electron and hole properties. The intuition of the method originates from successful processing and operation of simple Schottky-barrier SOI MOSFET's [2].



(a)

(b)

Fig. 1. (a) Schematic of the pseudo-MOS transistor in SOI structures. (b) Typical drain current versus drain voltage curves.

III. Experiment

Device-grade SIMOX wafers were fabricated by deep implantation of oxygen (100-mA current, 1.8×10^{18} cm^{-2} dose, 200-keV energy, 625°C) in p-type Si wafers (17-23 $\Omega \cdot$ cm), followed by high-temperature annealing (1320°C for 6 h in argon ambient). The thicknesses of the Si overlay and buried oxide were about 200 and 400 nm, respectively. In order to save material, small pieces of about 1-2 cm^2 were cut and etched on the borders. Measurements were performed with the Jandel resistivity system (tungsten-carbide probes of 0.4 mm diameter and 25-μm tip radius). The influence of charges at the top interface of the Si

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The authors are with the Laboratoire de Physique des Composants à Semiconducteurs (UA-CNRS), Institut National Polytechnique de Grenoble, ENSERG, 38016 Grenoble Cedex, France.

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