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INFLUENCE OF SERIES RESISTANCES AND INTERFACE COUPLING ON THE TRANSCONDUCTANCE OF FULLY-DEPLETED SILICON-ON-INSULATOR MOSFETs

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Abstract—A model is proposed to describe the variation of the transconductance in fully-depleted silicon on insulator MOSFETs as a function of the front/back gate biases, channel length and series resistances. The influence of series resistances on the static characteristics of short-channel transistors depends on the region of operation, via the front and back gate voltages, and is a maximum when both interfaces are inverted. Simple analytical expressions explain the gradual deformation of the transconductance curve and the lowering of the transconductance peak with increasing series resistances. The model is experimentally verified by associating external resistors to the transistor. It is shown that a major consequence of X-ray irradiations in short-channel SIMOX MOSFETs is the trapping of positive charges in the buried oxide, which causes activation of interface coupling effects and enhanced influence of series resistances.

NOTATION

The subscripts 1 and 2 relate to the parameters of the front interface and back interface, respectively. The superscript (^{0}) identifies "pure" transistor parameters which are unaffected by series resistances.

- $g_{m1,2}$ front/back channel transconductance
- g_{max1} maximum of g_{m1}
- g_{plat} value of g_{m1} in the plateau region
- $t_{ox1,2}$ front/back oxide thickness
- $C_{ox1,2}$ capacitances of the gate oxide and buried oxide
- C_{si} capacitance of the depleted Si film
- $C_{ss1,2}$ front/back interface state capacitance
- $G_{D_{1,2}}$ front/back channel conductance
- $I_{1,2}$ front/back Si–SiO_2 interface
- $I_{D_{1,2}}$ front/back channel current
- Z channel width
- L channel length
- $R_{1,2}$ front/back channel series resistances
- R_3 common series resistance for front and back channels
- R_{add} external resistance connected to the drain
- V_D drain voltage
- $V_{G_{1,2}}$ front/back gate voltage
- $V_{G_1}^{max}$ front gate voltage corresponding to g_{max1}
- $V_{T_{1,2}}$ front/back channel threshold voltage
- $V_{G_2}^{acc}$ value of V_{G_2} beyond which I_2 is always accumulated
- $V_{G_2}^{inv}$ value of V_{G_2} beyond which I_2 is always inverted
- $V_{T_2}^{acc}$ value of V_{T_2} when I_1 is accumulated
- $V_{T_2}^{inv}$ value of V_{T_2} when I_1 is inverted
- $V_{T_2}^{depl}$ value of V_{T_2} when I_1 is depleted
- V'_{T_1} value of V_{G_1} causing back channel activation
- $\mu_{1,2}$ front/back channel effective mobility
- μ_1^{acc} value of μ_1 when I_2 is accumulated
- μ_1^{inv} value of μ_1 when I_2 is inverted
- $\theta_{1,2}$ attenuation factor of front/back mobilities
- α capacitance coupling coefficient
- $\phi_{1,2}$ front/back surface potential
- Φ_F Fermi potential

1. INTRODUCTION

Fully-depleted silicon-on-insulator (SOI) MOS integrated circuits present improved performance in terms of speed and short-channel effects[1–4]. A fully-depleted structure is defined by the Si film being thinner than the depletion region controlled by either the front or the back gate (Fig. 1a). The total depletion of the film enables a strong *coupling* between the front and back interfaces which means that the front channel current can substantially be influenced by the back gate bias and vice versa. The interface coupling has been accounted for in the modeling of the threshold voltage[5] and subthreshold slope[6,7]. A model of the transconductance has been proposed recently [7] for the case of *ultra-thin* SOI films, where the minority carrier distribution can spread over the whole film.

In this paper, we present complementary models of the transconductance for *moderately* thin films. Such a film is still fully-depleted but the minority carriers are essentially confined at the front and/or back interfaces, the *volume inversion*[8] being negligible.

The next section deals with an ideal/simplified transconductance model which works in long-channel MOSFETs and illustrates the basic interface coupling effects. Described in Section 3 is the more complex case of short-channel MOSFETs where the transconductance is strongly affected by the series resistances. The model is validated in Section 4 by experiments consisting of an external adjustment of series resistances. A practical application, discussed in Section 5, is the