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ULTIMATE MOSFETs ON SOI: ULTRA THIN, SINGLE GATE, DOUBLE GATE, OR GROUND PLANE

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We tentatively present possible architectures of Silicon On Insulator (SOI) transistors for the final stages of the scaling of silicon microelectronics. The scaling trends for conventional partially depleted and fully depleted SOI MOSFETs are critically examined. A ground plane can considerably attenuate short-channel effects. The manufacturability of extremely thin MOSFETs is demonstrated. Based on quantum calculations, we discuss the merits of double-gate transistors with volume inversion.

1. Introduction

It was a long process to bring Silicon On Insulator (SOI) technology on the roadmap but SOI will most likely stay there until the 'end'. The attractiveness of SOI for the commercial market results from superior capabilities in terms of performance (higher speed, lower power consumption) and scalability. It is admitted that SOI integrated circuits are more effective for extending the frontiers of the Si-based micro- and nano-electronics. As a matter of fact, one can speculate that SOI transistors will be the unique survivors of the CMOS technology.

The aim of this paper is to take a critical look at the different configurations envisioned for the ultimate generations of SOI MOSFETs. The analysis will be conducted based on preliminary experimental data, quantum considerations, and numerical simulations. In section 2, we review the scaling philosophy for 'conventional' SOI transistors, which naturally will guide us to the concept of the ground plane (section 3). Section 4 is dedicated to the investigation of ultra-thin transistors where the body thickness is reduced to a few monolayers of silicon. Finally, the merits of double-gate MOSFETs will be discussed in section 5.

2. Scaling Trends of Conventional SOI MOSFETs

Numerous scaling rules, more or less stringent, have been elaborated for bulk Si MOSFETs.[1,2] They all converge on the necessity to reduce the junction thickness and increase the doping level, which adversely affects the junction capacitances and circuit speed. At this point, the topological advantage of thin-film SOI becomes obvious: the junction capacitance, defined by the film thickness, is naturally low.[3] In addition, SOI is more versatile than bulk Si because there are supplementary