A Review of the Pseudo-MOS Transistor in SOI Wafers: Operation, Parameter Extraction, and Applications

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***Abstract*—The pseudo-MOS transistor (Ψ-MOSFET) is a surprising and useful technique for the rapid evaluation of SOI wafers, prior to any CMOS processing. We review the static and dynamic modes of operation as well as the main models and methods for electrical parameter extraction. Selected numerical simulations are presented in order to clarify the optimal conditions of operation. Finally, practical applications are exemplified which illustrate the efficiency of the Ψ-MOSFET technique for *in situ* characterization of SOI technologies and processes.**

***Index Terms*—Characterization, pseudo-MOSFET, SOI, SOI technology, unibond.**

I. INTRODUCTION

HALF A century ago, the Shockley group at Bell Laboratories was frantically attempting to prove the concept of the field-effect transistor. The revolutionary idea promoted by Shockley was that a (metal) gate, placed in the close vicinity of a semiconductor material, can induce a change in the surface conductivity. In order for such a conductivity modulation to be discernible, a very thin semiconductor slab was needed as well as two pressure probes serving as drain and source contacts. The first transistor consisted of a thin Ge slab, a gate SiO_2 insulator, and an Au gate. After a series of more or less successful attempts and manipulation hazards, Bardeen, Brattain, and Shockley ended up demonstrating transistor action and brilliantly elucidating its secret: the predictable MOS transistor turned out to operate as a … bipolar transistor [1], [2].

The MOSFET had to experience another decade of gestation before being born. Shockley's task would have been far easier if, at that time, he had the chance to be aware about silicon-on-insulator (SOI) structures which intrinsically fulfill the conditions requested for MOSFET operation. Any SOI material has indeed a natural, upside-down MOS configuration (Fig. 1) [3]–[5]. The silicon film represents the transistor body and the buried oxide serves as the gate insulator. The thick Si substrate plays the role of the gate and can be biased through a metal support to induce a conducting channel at the interface between the film and oxide. Depending on the positive or negative "gate" bias, an inversion or accumulation channel can be activated.

The source and drain are readily formed by applying low-pressure probes on the film surface. Typical $I_D(V_G, V_D)$ characteristics are reproduced in Fig. 2. This fascinating device was named pseudo-MOSFET (Ψ-MOSFET) [3] or point-contact transistor [4]. The Ψ-MOSFET idea germinated while performing Hall effect measurements in bare SOI samples, where the Hall voltage showed a dependence on substrate bias. Since its early demonstration [3], [4], the Ψ-MOSFET has served for *in situ* characterization and optimization of SOI wafers.

Reviewed in this paper are the set-up and operation modes of the Ψ-MOSFET in Section II, the appropriate methods for parameter extraction in Section III and recent numerical simulations in Section IV. Examples of application for either SOI material screening/inspection or detailed evaluation and comparison of various SOI wafers will be highlighted in Section V.

II. Ψ-MOSFET SETUP AND OPERATION

The Ψ-MOSFET is basically a wafer-scale experiment. This implies no leakage current through the oxide (i.e., pipe-free material such as wafer-bonded SOI) or around edges. In practice, Si islands of variable size (from 1 mm^2 to 1 cm^2) are defined by etching off their borders (Fig. 1). This procedure has the advantage of enabling a quick check of the wafer uniformity and of the density of oxide pipes (by measuring the leakage current through the oxide, see Section V-E.) Also, the sample surface needs to be oxide free and clean in order to avoid the degradation of Ψ-MOSFET characteristics.

Any two-probe system can be used. However, pressure-adjustable probes show that best results are obtained for about 50 g pressure: As the series resistance is drastically reduced, the mobility degradation factor θ tends to an intrinsic saturation value θ_0 [see (3) and Fig. 11(a)] and the transconductance peak reaches a maximum [Fig. 3(b)] [3], [5]. For 10 g, the probes penetrate roughly 10 nm into the Si film, but the induced damage extends deeper. As for other probing techniques (four-point probes, spreading resistance, etc.), it is speculated that this damage is causing the necessary conversion of the Schottky contacts into ohmic contacts for both electron and hole flows.

The probe's interdistance can vary from 100 μm up to 1–5 mm. Geometrical effects related to the probe size or probe proximity near the sample borders will be discussed in Section IV.

Most measurements are performed with an HP-4155A semiconductor parameter analyzer, at low-drain bias ($V_D \simeq 100$ mV) and in the dark. A "fast" $I_D(V_G)$ curve is obtained by

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