Self-consistent solution of the 2D Schrödinger-Poisson equations in Multiple-Gate SOI MOSFETs

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1. Abstract

Gate lengths bellow 100nm produce an increasing of the short channel effects. Multiple-gates offer a solution to this problem although new challenges have to be faced. Quantum effects are dominant in the electrostatic of these devices. Therefore, accurate simulations need the self consistent solution of Poisson and Schrödinger equations in two dimensions. In this work we analyze a variety of multiple-gate SOI MOSFETs. Moreover our simulator allows the study of rounded corners on the silicon substrate and on the oxide.

2. Introduction

Traditional bulk MOSFETs faces different problems when the channel length is reduced to a few nanometers. A high impurity density is necessary to keep short channel effects (SCEs) under control. As a consequence, the carrier mobility is reduced and the device performance is degraded. Moreover, in such short channel devices, the random impurity effects are not negligible since they produce a dispersion of fundamental parameters like the threshold voltage. To deal with this situation, an undoped channel is the best choice. However, this solution is not appropriate for a bulk MOSFET due to the increase of penetration of the drain electric field lines in the channel region. To solve this problem new structures such as FinFETs, Trigates, or Gate All Around (GAA) MOSFETs have been proposed. All of them have in common that take advantage of the SOI technology and that their gates are located in different planes. This implies that these new devices are essentially three dimensional. In order to understand these structures it is mandatory to take into account the quantum effects due to their reduced dimensions. In this work we have carried out a thorough study of the electrostatic of these devices. To do so, we have self-consistently solved the Poisson and Schrödinger equations in two dimensions (2D), specifically in a plane perpendicular to carrier transport (from source to drain). This simulator is prepared to analyze different structures such as: FinFETs, Trigates, GAA, and Pi and omega-gate MOSFETs. Figure 1 shows the geometry of these devices where *w* is the silicon width, *h* is the silicon height, t_{ox} is the gate oxide thickness, t_{oxb} the buried oxide thickness and *r* is the corner radius.

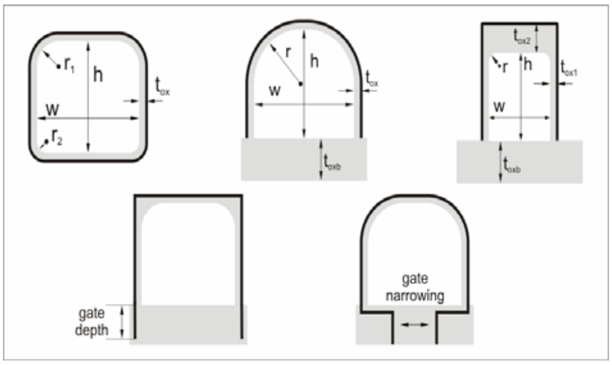

Fig.1: *Geometry of the different structures studied.*

Different geometries can be considered and the simulator offers the possibility of specifying the curvature of the silicon substrate corners, and the surrounding oxide details, independently. This fact is quite useful to evaluate the influence of the corner effects.

3. Simulation and results

To get a fast convergence, both equations have been solved using the predictor-corrector scheme proposed by Trellakis et al [1]. This algorithm has been proved as reliable and robust in all the structures considered in our study as far as enough number of eigenvalues and eigenfunctions are included in the quantum electron density (QED) calculation.

In this work, electrostatic characteristics of nanowire multiple-gate FETs have been explored taking into account quantum effects. In all the devices simulated we have considered that $H_{Si}=W_{Si}=20$nm, $T_{ox}=2$nm and $V_G=1$V. The substrate is undoped and a metal gate with workfunction $\phi_m=4.63$eV has been employed. As a first result we show in Figure 2 a Trigate structure. On the left side the classical simulation is shown while on the right side the quantum effects have been included. As can be readily observed, the classical electron distribution is concentrated at the Si-SiO$_2$ interface with a maximum at the corner of $n_{max}=6.65\times10^{20}$cm^{-3}. On the other hand, a more realistic simulation including the quantum effects shows an electron distribution separated from the interface. An interesting result is that the maximum of the QED is now $n_{max}=9.39\times10^{19}cm^{-3}$ which represents a considerable reduction compared to the classical case. Furthermore, if the total electron density in the silicon area is calculated:

$$Q_{tot} = \int_S n(x,y)\,dxdy$$

it is observed that $Q_{tot,clas}=8.13\times10^{7}cm^{-1}$ and $Q_{tot,quant}=5.29\times10^{7}cm^{-1}$. Therefore, classical simulations clearly overestimate the charge involved in the current evaluation.

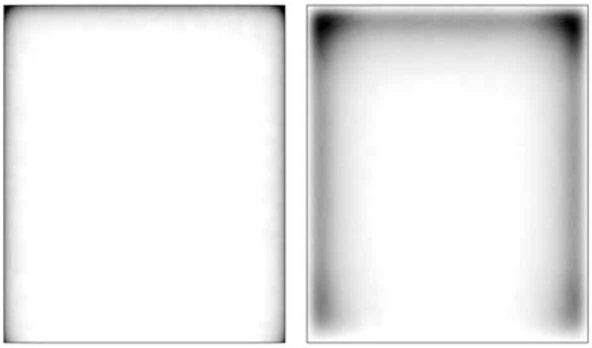

Fig.2: *Classical (left) and quantum (right) electron density in a Trigate FET.*

Corner effects are produced by the coupling between different gates which produces an electrostatically favourable area for the flow of carriers [2]. An efficient way to avoid corner effects is by using corner rounding and undoped channels. To deal with a rounded geometry our simulator employs finite elements instead of finite differences. Figure 3 shows the results obtained when the corners of a Trigate FET, similar to that one used in Fig. 2, are rounded. In this case the corners of the silicon slab have been rounded with a curvature radius of 10nm (the *r* value can be arbitrarily fixed).

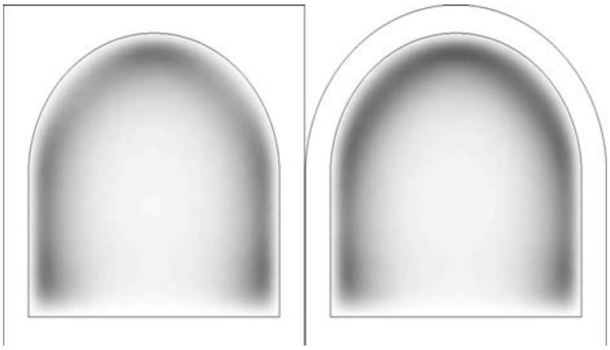

Fig.3: *Quantum electron density in a Trigate FET with silicon corner rounding. Left: The gate has a square cross section and the gate oxide is not uniform. Right: The gate contact follows the silicon producing a uniform gate oxide.*

On the left side, the gate presents a square section producing an oxide with a variable thickness. As a consequence the electron density is reduced on the proximity of the corners due to an increase of T_{ox}. On the right side, the gate contact follows the silicon profile and the oxide thickness is constant all along the gate. As can be observed in the figure a uniform electron distribution is obtained. As a comparison, the total charge on Fig.3-left is $Q_{tot}=1.65\times10^{7}cm^{-1}$ and for the Fig.3-right is $Q_{tot}=1.9\times10^{7}cm^{-1}$ which results in a higher charge for the uniform gate oxide. It is interesting to highlight that in Fig 3 the maximum of the QED is $n_{max}=1.5\times10^{19}cm^{-3}$ which represents 1/6 of the value obtained in Fig. 2 with a square cross section.

Unlike the double-gate or the GAA structure, the Pi-gate SOI MOSFET can readily be manufactured from a conventional SOI CMOS fabrication process [3]. The Pi and omega-gate structures can be obtained by extending the lateral gates under the body of the device. The extension of the gates in the buried oxide (L_{ext}) will determine the electron density present in the device. Figure 4 shows the results obtained when both devices are simulated with L_{ext} =8nm.

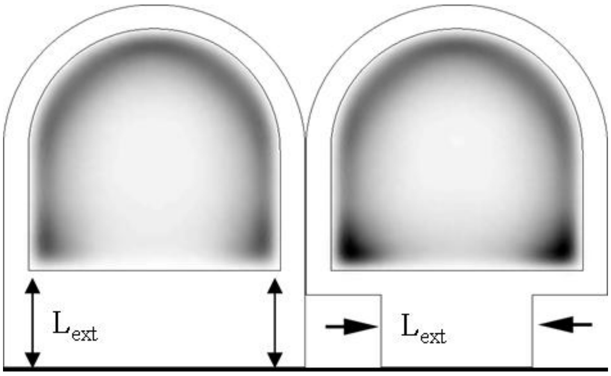

Fig.4: *Quantum electron density in a Pi and omega-gate FET.*

When the value of L_{ext} increases, the behaviour of both devices resembles more and more to a GAA FET. Due to the corners present in the omega-gate FET its value of n_{max} is considerably higher ($n_{max}=2.46\times10^{19}cm^{-3}$) than the value obtained for the Pi-gate ($n_{max}=1.68\times10^{19}cm^{-3}$). Moreover, also a higher value of Q_{tot} is obtained for the omega-gate.

4. Conclusions

A complete numerical simulator that includes quantum effects has been developed. It allows us the study and comparison of the electrostatic characteristics of a wide variety of multiple-gate SOI MOSFETs including corner rounding.

Acknowledgments

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