



INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

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D2.3 Report on Scientific Exchange Visits performed during the first reporting period (M1-M14)

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Project coordinator organisation: University of Granada, Spain

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Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

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1. Introduction

One of the main goals of EUROSOL+ is the promotion of exchange of knowledge and experience between research groups working on materials, devices, circuits and electronic end-user applications. This idea tries to support the interaction and scientific exchange between partners through staff mobility, staff exchanges, and joint execution of research projects.

To get this goal the network supports a number of short scientific exchanges.

It was initially proposed 10 visits per year with duration between one week and one month which means 54 weeks in total with a maximum of 1400€/week. Funding only covers for travel and subsistence expenses.

The results of this task during the first 14 months of EUROSOL+ are summarized in the next pages.

2.- Scientific Visits Second Semester of 2008

Origin (Person and Affiliation):

Carlos Sampedro; Departamento de Electrónica, Universidad de Granada

Destination (Responsible and Affiliation):

Antonio García Loureiro; Supercomputation Center, Universidad de Santiago de Compostela, Spain

Start Date: 31/08/2008

End Date: 15/09/2008

Topic of the Visit: Parallelization of the Multi Valley – Effective Conduction Band-Edge code. The code was tuned since previous work had been already performed in the frame of Spanish projects.

Origin (Person and Affiliation):

T. E. Rudenko; Institute of Semiconductor Physics; National Academy of Sciences of Ukraine, Kyiv, Ukraine

Destination (Responsible and Affiliation):

Denis Flandre; Université Catholique de Louvain, Louvain-la-Neuve, Belgium

Start Date: September 29th 2008

End Date: October 29th 2008

Topic of the Visit: Modeling and parameter extraction of nanoscaled devices based on ultra-thin-body SOI

Origin (Person and Affiliation):

Bastien Giraud; PhD student ISEP, France

Destination (Responsible and Affiliation): Olivier Thomas, Research Engineer at Design department of CEA/LETI at Grenoble, France.

Start Date: November 3rd 2008

End Date: November 28th 2008

Topic of the Visit: Evaluate the 32nm FDSOI technology for designing SRAM memory circuits. The PhD student will work on SRAM decoder circuits. He will address the various architectures ways to reduce dynamic and static power consumption taking into account the FDSOI device architecture

Origin (Person and Affiliation):

Alexei Nazarov; Institute of Semiconductor Physics, National Academy of Sciences of Ukraine, Kyiv, Ukraine

Destination (Responsible and Affiliation):

J.P. Colinge; Tyndall National Institute, Cork, Ireland

Start Date: November 17th 2008

End Date: December 12th 2008

Topic of the Visit: Research and analysis of electrical parameters FinFETs with buried nitridelayer. Estimation of influence of buried interface and charge in buried dielectric on main electrical properties of the FinFET.

Origin (Person and Affiliation):

Benjamín Iñiguez; URV Tarragona, Spain

Destination (Responsible and Affiliation):

Denis Flandre; Université Catholique de Louvain, Louvain-la-Neuve, Belgium

Start Date: December 2008

End Date: 1 week

Topic of the Visit: Compact modeling of thin-film SOI MOSFETs, including FinFETs.

3.- Scientific Visits First Semester of 2009

Origin (Person and Affiliation): Noel Rodríguez; UGR, Granada, Spain

Destination (Responsible and Affiliation): Sorin Cristoloveanu; IMEP
Grenoble, France

Start Date: January 22nd 2009

End Date: February 12th 2009

Topic of the Visit: Perfection of the electrical characterization skills of the applicant at IMEP facilities

Origin (Person and Affiliation): Carlos Sampedro Matarín; UGR, Granada, Spain

Destination (Responsible and Affiliation): Antonio García Loureiro;
Supercomputation Center, Universidad de Santiago de Compostela, Spain

Start Date: February 16th 2009

End Date: February 19th 2009

Topic of the Visit: Parallelization of the Multisubband Ensemble Monte Carlo code. The code was run at the CESGA supercomputation center.

4.- Activity Report

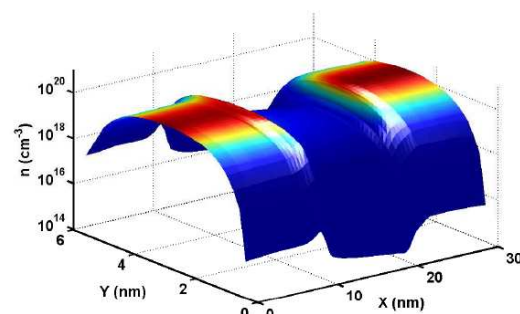
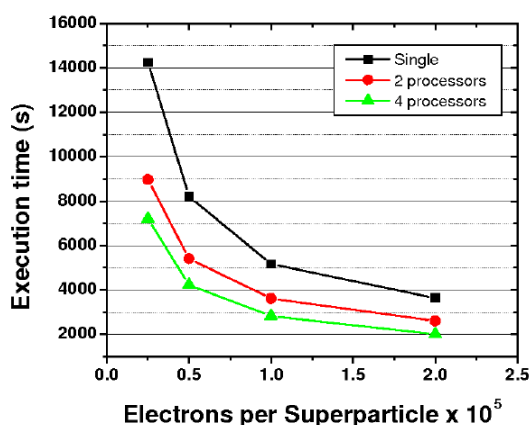
Member: Dr. Carlos Sampedro Matarin (UGR)

Destination: Universidad de Santiago de Compostela, Spain (USC)

Date: 31/08/2008 – 15/09/2008

Description of the work:

The use of device simulators including quantum effects is mandatory for the study of ultra-short channel MOS transistors. However, the complexity and computational requirements produce an important increase of the execution time. In this scenario, parallelization and grid computing techniques can speed up simulation tools to obtain accurate predictions based on quantum approximations in an affordable time. The goal of this visit was to apply the expertise on parallelization techniques of the USC group to the quantum corrected ensemble Monte Carlo codes (EMC) developed at UGR. Two approximations were studied: the first one includes quantum effects correcting the electrostatic potential with the multi-valley effective conduction band-edge method (MV-ECBE). The second one is based on the multi-subband (MS) approach where the 1D Schroedinger equation is solved for each considered slice from source to drain. During my visit, the parallelization of the MV-ECBE code was tuned since previous work had been already performed in the frame of Spanish projects. The MS simulator parallelization was also started with some important routines (i.e. Schroedinger solver) and first results were presented on EUROSIO 2009 and CDE 2009 conferences (see figures for speed-up comparison for MV-ECBE schemes and electron concentration profile in benchmark DGSOI devices). The collaboration continues by the development of new parallel routines using OPENMP.



Member: T. Rudenko (ISP NASU, Ukraine)
Destination: UCL (Louvain-la-Neuve, Belgium)
Date: 29/09/2008 – 29/10/2008

Description of the work:

During the visit of T. Rudenko to UCL (LLN, Belgium) from 29.09.08 to 29.10.08 the electrical characteristics of ultra-thin body (UTB) SOI MOSFETs with the TiN/HfO₂ gate stack and standard and ultra-thin buried oxide (BOX) fabricated at CEA-LETI have been studied. In particular, using the analysis of the transconductance, gate-to-channel capacitance and carrier mobility extracted with split CV technique for long-channel devices for various substrate biases, it has been found that the electron mobility at the back interface in the studied UTB SOI MOSFETs with high-k gate dielectric is significantly (nearly twice) higher than that at the front interface, which has been attributed to different front (TiN/HfO₂) and back (Si/SiO₂) gate stacks. No degradation of the transconductance and carrier mobility has been found for thin BOX devices.

A large scatter in the drive current, transconductance and carrier mobility has been observed in the studied UTB devices at zero substrate bias. This scatter was more pronounced for thin BOX devices. Based on the combined analysis of the capacitance and mobility results for zero substrate bias, it has been concluded that the observed large scatter in the effective mobility at zero substrate bias is rather related to variations in the BOX charge, rather than to variations in the Si film thickness. An additional factor resulting in a large scatter in the drive current and transconductance, especially in the short-channel devices, is a large scatter in the series resistance, which also may be related to the variations in the BOX charge, due to modulation of the conduction in the non-overlapped drain/source extension regions.

It has been found that thick and thin BOX devices reveal different dependencies of the threshold voltage and gate-to-channel tunnelling current on the back gate bias, which is attributed to different potential distributions across the device structure for thick and thin BOX.

Some of the results obtained during this visit are presented in the work entitled "Transconductance and mobility behaviours in UTB SOI MOSFETs with standard and thin BOX" submitted to EUROSOL 2009 Conference".

Member: Bastien Giraud (ISEP, Paris France)

Destination: CEA/LETI at Grenoble, France

Date: 3/11/2008 – 28/11/2008

Description of the work:

The visit was focused on RAM Decoder Circuits in 32nm FDSOI technology.

The main objectives of the visit were:

- 1.- Study of FD-SOI technologies and related effects.
- 2.- Bibliography on state-of-the-art SRAM memory decoders.
- 3.- Review of low power SRAM memory decoders.
- 4.- Comparative analysis of the different decoder circuit architectures.
- 5.- Power and performance optimization.
- 6.- Optimized circuit Design.

The conclusions of this work:

3 main criteria (delay, power and area) have to be taken into account.

Several improvement techniques have been exposed. They basically consist in:

- Matrix level improvements (predecoders, such divided WL, selective precharge of decoder outputs).
- Using new circuits (such as drivers, boost word drivers).
- Circuit level improvements (such as pulse WL, half-swing WL).

Member: Prof. O. Nazarov (Lashkaryov Institute of Semiconductor Physics, NAS of Ukraine, Kyiv, Ukraine)

Destination: Tyndall National Institute (Cork, Ireland)

Date: 17/11/2008 – 12/11/2008

Description of the work:

The goal of the visit consists in carrying out measurements of nanoscaled SOI FinFETs and MOSFETs fabricated with buried nitride dielectric and analysis effect of buried dielectric with high dielectric constant on gate control of channel in the FinFETs. Additionally it was performed study of charging of the buried dielectric at back gate voltage applied and special measurements of carrier mobility at bottom channel using split CV method.

It was demonstrated that the buried dielectric possesses large positive charge, however good gate control of channel in the FinFETs allows to escape from the charge influence both for n-type inversion mode and p-type accumulation mode devices. Memory effect in the buried dielectric was also studied.

Member: Prof. Benjamin Iñiguez (Universitat Rovira I Virgili, URV, Tarragona, Spain)

Destination: UCL (Louvain-la-Neuve, Belgium)

Date: 3/02/2009 – 7/02/2009

Description of the work:

During his visit, Prof Iñiguez had several meetings with UCL researchers (professors, postdocs and students) to discuss joint work on the compact modelling of thin-film SOI MOSFETs, including UTB (Ultra-Thin Body) SOI MOSFETs, DG (Double-Gate) SOI MOSFETs and FinFETs. In particular, some of the discussions focused on possible explanations of specific effects recently found in current and capacitance characteristics in UTB and Ground-Plane SOI MOSFETs, due to coupling between gates. In order to intensify the collaboration between the two groups to model these effects, it was agreed that experimental measurements on these devices will be sent to URV.

Prof. Iñiguez and UCL researchers also agreed on a joint plan to characterize and model Schottky-Barrier (SB) SOI MOSFETs. The two groups will jointly target SB devices fabricated in the framework of NANOSIL. Some modeling ideas were already discussed during Prof. Iñiguez's visit.

Finally, Prof. Iñiguez discussed with some UCL researchers about the results of a protein detector based on a Nano-Interdigitated Gate SOI MOSFET. A paper presenting the results will be soon sent for publication.

Member: Noel Rodriguez-Santiago, PhD

From: University of Granada (Spain)

Hosting institution: Institut de Microélectronique Electromagnetisme et Photonique (IMEP-MINATEC), Grenoble (France)

Dates: From 22nd January 2009 to 12th February 2009

REPORT

After three weeks of stay in Grenoble three main objectives were accomplished: Improvement of measurements skills of the visitor inside IMEP facilities, exchanging scientific results, defining future research activities in collaboration between UGR and IMEP.

Improvements of skills: One of the main objectives of this visit was the improvement of the electrical characterization skills of the visitor researcher in the heart of one of the most prestigious European labs in device characterization. This has special interest due to the future placement of an electrical characterization lab at UGR. Traditionally, the nanoelectronics research group at UGR has been focused in advanced modelling and simulation (with emphasis in transport) where great achievements in terms of scientific production and dissemination of results have been obtained; Now a new research line has been opened dedicated to device characterization to expand the future scope of the group. Several unique techniques will be imported from IMEP. In particular, during this stay the Pseudo-MOSFET characterization technique was considered in detail. This unique method, developed in IMEP lab, allows wafer level characterization before any CMOS processing in a cheap, simple and reliable way.

The other characterization topic considered was related to the use and operation of advanced equipment such as the impedance analyzer, LCR and semiautomatic probe stations. Standard equipment (parameter analyzer, manual probe stations) was already used by the visitor during a previous stay in IMEP during his PhD. Due to the unique environment where IMEP is located (beside LETI and surrounded by important semiconductor companies) several meetings were scheduled with labs technicians in order to get the best possible feedback for the characterization lab that is going to be set up at UGR.

Exchanging scientific results: During this visit the results corresponding to previous research collaborations established between both institutions (UGR and IMEP) were put in common. This research is mainly related to the development of improved models for the pseudo-transistor characterization. The initial pseudo-MOSFET technique was conceived almost ten years ago when the silicon thickness of the SOI devices was several times the present one. The previous pseudo-transistor models developed for thick layers are no longer valid because some of the assumptions made for the derivations are inaccurate for thin silicon layers. About one year ago a collaboration between UGR and IMEP was started to improve the existing models. The final results were discussed during the stay and the achievements of the collaboration are going to be reflected in two papers sent to high impact international journals.

Defining future research collaborations: During the three weeks of stay new research collaboration projects were also scheduled. These new topics are mainly related to two different activities based on advance characterization and device design. Because industrial partners are involved in these research tasks the technical aspects of the work are not going to be discussed in the current report.

Member: Dr. Carlos Sampedro Matarin (UGR)

Destination: Universidad de Santiago de Compostela, Spain (USC)

Date: 16/02/2009 – 19/02/2009

Description of the work:

In this second visit, we continued the work on the parallelization of the Ensemble Monte Carlo Multi Subband simulator (EMC-MS). The first part of the code to be parallelized has been the 1D Schroedinger equation. Thanks to the independent solution for each considered slice, the application of parallel techniques is straightforward. There were also applied profiling techniques to characterize the computational effort corresponding to each routine. We identified then, the suitable routines for parallelization and the fraction of the computational effort that can be speeded-up by using OPENMP. As a result, more than 95% of the code can be improved. We started then with the parallelization of the routines devoted to the scattering table calculation. Finally, the code was also tested in different supercomputing facilities including the Finis-Terrae in USC with 2500 64-bit CPUs and 19000 Gbytes RAM memory. Different GRID infrastructures corresponding of the Galicia supercomputation centre (CESGA) were also used to determine the performance of the simulator in different computing architectures.

