



INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

Grant Agreement n° 216373

D3.1 Distinguished Lecturers List

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Project coordinator: Prof. Francisco Gámiz, UGR

Project coordinator organisation: University of Granada, Spain

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Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

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1.- Introduction.

Training activities for young researchers are fundamental since they help to retain qualified young scientists and engineers within Europe, thus guaranteeing the man-power of tomorrow. Up to now, EUROSUI network has organized different one-day training courses. They were fully successful. We want to be now much more ambitious, and we want to create a durable training structure on SOI technology (from materials to end-user applications), whose main goal is to manage the training of European young researchers on SOI, with the development of different initiatives. The first of these initiatives is to establish a EUROSUI Distinguished Lecturers list.

The list of EUROSUI Distinguished Lecturers has been elaborated in two phases. In a first stage, a public request was made by Prof. Andres Godoy to all the members of EUROSUI network, asking them the names of well-known specialists in the field of SOI technology, and the particular topic in which this person is supposed to be an expert. We added to this list, the name of the lectures who have already participated in the four short courses already organized by EUROSUI in the previous years. This gave us a list with more than fifty names. The second stage consisted on the selection by the Management Board of EUROSUI+ of the final Distinguished Lecturers List among the previous list, by voting to each candidate 0, 1 or 2. The final list is formed by the most voted names. This list will be re-considered after each Management Board (MB) meeting. As this list is going to be published on line on our Website, Prof. Engstrom (Chalmers) advised that it would be convenient to ask for the permission of the selected people in order to include them in the list. The MB agreed with this point, and although the Deliverable has been submitted to the Commission, the list is not going to be published until we have the clearance of all the lecturers.

TOPIC	SOI MATERIALS		
Name	Affiliation	e-mail	Subtopic
Jean-Pierre Colinge	Tyndall National Institute	jean-pierre.colinge@tyndall.ie	
Sorin Cristoloveanu	Institute of Microelectronic	sorin@enserg.fr	
Carlos Mazuré	Soitec	carlos.mazure@soitec.fr	Advanced SOI materials
K. Mitani	SEH	k.mitani@seh.co.jp	
Alex Zaslavsky	Brown Univ, USA	Alexander_Zaslavsky@brown.edu	Innovative SOI and GeOI devices
Thomas Ernst	LETI	thomas.ernst@cea.fr	Nanowires and other innovative SOI devices
Stefan Bengtsson	Chalmers	stefan.bengtsson@chalmers.se	Innovative SOI materials
Laurent Clavelier	CEA-LETI	laurent.clavelier@cea.fr	Advanced Substrates
Bruno Ghyselen	Soitec	ghyselen@soitec.fr	Advances in SOI materials

TOPIC	DEVICES. CHARACTERIZATION		
Name	Affiliation	e-mail	Subtopic
Sorin Cristoloveanu	Institute of Microelectronic	sorin@enserg.fr	
E. Simoen	IMEC	simoen@imec.be	Low frequency noise characterization in SOI materials and devices
J.P. Raskin	UCL	raskin@emic.ucl.ac.be	Wideband characterisation of SOI materials and devices
Dieter K. Schroder	Arizona State University	schroder@asu.edu	

TOPIC	DEVICES. FABRICATION TECHNOLOGY		
Name	Affiliation	e-mail	Subtopic
Malgorzata Jurczak	IMEC	Malgorzata.Jurczak@imec.be	Multigate MOSFET Technology
A. Vandooren	Freescale	anne.vandooren@freescale.com	Multiple gates and strained films for SOI MOSFETs : from technology to characterization and applications

TOPIC	DEVICES. PHYSICS		
Name	Affiliation	e-mail	Subtopic
Jean Pierre Colinge	Tyndall National Institute	jean-pierre.colinge@tyndall.ie	
S. Takagi	Univ of Tokyo	takagi@ee.t.u-tokyo.ac.jp	Transport and quantum effects in SOI devices
T. Hiramoto	Univ of Tokyo	hiramoto@nano.iis.u-tokyo.ac.jp	Transport and quantum effects in SOI devices
Bogdan Majkusiak	Warsaw University of Technology	B.Majkusiak@acn.waw.pl	Physics of the Multigate MOS System

TOPIC	SIMULATION AND MODELLING		
Name	Affiliation	e-mail	Subtopic
Asen Asenov	University of Glasgow	asenov@elec.gla.ac.uk	Monte Carlo Simulation for variability issues
Francisco Gámiz	Universidad de Granada	fgamiz@ugr.es	Characterization and simulation issues for SOI devices
Benjamín Íñiguez	Universitat Rovira i Virgili	Benjamin.iniguez@urv.cat	Compact modeling techniques for thin-film SOI MOSFETs, including Multi-Gate MOSFETs
Jerry Fossum	University of Florida	fossum@tec.ufl.edu	SOI device modelling
D. Esseni	Univ. Udine	esseni@uniud.it	Characterization and simulation issues for SOI devices

TOPIC	RELIABILITY OF SOI DEVICES AND CIRCUITS		
Name	Affiliation	e-mail	Subtopic
Sorin Cristoloveanu	Institute of Microelectronic	sorin@enserg.fr	Specific SOI effects
Véronique Ferlet	CEA	veronique.ferlet@cea.fr	Radiation effects in SOI devices
Ron Schrimpf	Vanderbilt Univ, USA	ron.schrimpf@vanderbilt.edu	Radiation effects in SOI devices

TOPIC	PHYSICS. ADVANCED DEVICE CONCEPTS		
Name	Affiliation	e-mail	Subtopic
Sorin Cristoloveanu	Institute of Microelectronic	sorin@enserg.fr	Advanced multiple-gate transistors
H.S.P. Wong	Stanford University	hspwong@stanford.edu	

TOPIC	SOI CIRCUIT DESIGN		
Name	Affiliation	e-mail	Subtopic
Philippe Flatresse	ST Microelectronics	philippe.flatresse@st.com	
Amara Amara	ISEP, France	amara.amara@isep.fr	Low Power circuit design
Marc Belleville	CEA-LETI	marc.belleville@cea.fr	Benchmarking with Bulk
Pierre Fazan	Innovative Silicon	pfazan@z-ram.com	ZRAM on SOI
Olivier Thomas	CEA-LETI	olivier.thomas@cea.fr	SRAM design in advanced technologies (PDSOI, FDSOI, Double-Gate FET, Multi-channel FET)
Gerhard Knoblinger	Infineon	gerhard.knoblinger@infineon.com	Multigate MOSFET Circuit Design
Serguei Okhonin	Innovative Silicon Inc.	serguei.okhonin@epfl.ch	Z-RAM Memory Technology
Bill Redman White	Univ. Southampton + Philips	bill.redman-white@nxp.com	Designing around SOI
Carlo Tinella	STMicroelectronics	carlo.tinella@st.com	SOI Circuits for RF applications
A. Dubreuil	DITOCOM	alain.dubreuil@ditocom.fr	Technology Issues in SOI RFIC

TOPIC	END USERS & INDUSTRIAL APPLICATIONS		
Name	Affiliation	e-mail	Subtopic
Jean Pierre Colinge	Tyndall National Institute	jean-pierre.colinge@tyndall.ie	Special applications
Piet Wessels	Philips	piet.wesseld@philips.com	Industrial SOI technologies & applications
N. Mitchell	Queens Univ. Belfast	n.mitchell@ee.qub.ac.uk	Non-CMOS applications for SOI (sensors, MEMS, power, photonics, etc)
P.Delatte	CISSOID	delatte@cissoid.com	SOI market and applications