



## INFORMATION AND COMMUNICATION TECHNOLOGIES

### COORDINATION AND SUPPORT ACTION

# EUROSOI+

## European Platform for Low-Power Applications on Silicon-On-Insulator Technology

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## D3.2 First Inventory of available training material and generation of web based training material

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Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

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## **1. Introduction**

As one of the aims of the network, during these months we have performed the elaboration of an inventory of the SOI related training material available among the different partners. To this end, several announcements were published on the website and in the monthly EUROSUI Newsletter requesting the participation not only of the members of the network but also of other members from the international SOI community.

We regard this task as very useful for our community, especially for the youngest in the field. A selection of this material is available to all partners through the website.

The creation of new didactic materials will be a concern during the whole life of the network.

## 2. Books.

### General Textbooks on SOI

#### **Silicon-on-Insulator Technology: Materials to VLSI**

*Colinge, J.-P.*

*3rd ed., 2004, 384 p., Hardcover*

*Kluwer/Springer ISBN: 978-1-4020-7773-9*

#### Table of contents

1. Introduction
2. SOI Materials
3. SOI Materials Characterization
4. SOI CMOS Technology
5. The SOI MOSFET
6. Other SOI Devices
7. The SOI MOSFET in a Harsh Environment
8. SOI Circuits. Index

#### **Electrical Characterization of Silicon-on-Insulator Materials and Devices**

*Cristoloveanu, Sorin, Li, Sheng*

*1995, 400 p., Hardcover*

*Kluwer/Springer ISBN: 978-0-7923-9548-5*

#### Table of contents

1. Introduction
  2. Methods of Forming SOI Wafers
  3. SOI Devices
  4. Wafer Screening Techniques
  5. Transport Measurements
  6. SUS Capacitor Based Characterization Techniques
  7. Diode Measurements
  8. Transistor Characteristics
  9. Transistor Based Characterization Techniques
  10. Monitoring the Transistor Degradation
- Index.

## Books focused on a particular SOI topic

### **FinFETs and Other Multi-Gate Transistors**

*Colinge, J.-P. (Ed.)*

*2008, XVI, 340 p., Hardcover*

*Springer ISBN: 978-0-387-71751-7*

#### Table of contents

1. The SOI MOSFET: From Single Gate to Multigate
2. Multigate MOSFET Technology
3. BSIM-CMG: A Compact Model for Multi-Gate Transistors
4. Physics of the Multigate MOS System
5. Mobility in Multigate MOSFETs
6. Radiation Effects in Advanced Single- and Multi-Gate SOI MOSFETs
7. Multi-Gate MOSFET Circuit Design

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### **Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications**

*Sakurai, Takayasu, Matsuzawa, Akira, Douseki, Takakuni*

*2006, XV, 411 p., Hardcover*

*Kluwer/Springer ISBN: 0-387-29217-9*

#### Table of contents

1. Introduction
2. FD-SOI Device and Process Technologies
3. Ultralow-Power Circuit Design with FD-SOI Devices
4. 0.5-V MTCMOS/SOI Digital Circuits
5. 0.5-1V MTCMOS/SOI Analog/RF Circuits
6. SPICE Model for SOI MOSFETs
7. Applications
8. Prospects for FD-SOI Technology

**SOI Circuit Design Concepts**

*Bernstein, Kerry, Rohrer, Norman J.*

*2000, 240 p., Hardcover*

*Kluwer/Springer ISBN: 0-7923-7762-1*

## Table of contents

1. The Time for SOI
2. SOI Device Structures
3. SOI Device Electrical Properties
4. Static Circuit Design Response
5. Dynamic Circuit Design Considerations
6. SRAM Cache Design Considerations
7. Specialized Function Circuits in SOI
8. Global Chip Design Considerations
9. Future Opportunities in SOI.

**SOI Design: Analog, Memory and Digital Techniques**

*Marshall, Andrew, Natarajan, Sreedhar*

*2002, 416 p., Hardcover*

*Kluwer/Springer ISBN: 0-7923-7640-4*

## Table of contents

1. Overview
  2. SOI Materials
  3. Components
  4. SOI Modeling
  5. Layout for SOI
  6. Static SOI Design
  7. Dynamic SOI Design
  8. SOI SRAMs
  9. SOI DRAMs
  10. SOI Analog Design
  11. Global Design Issues
  12. Low Power Design
  13. SOI in Development
- Appendix 1: Internet Sites (issue 1.0)  
Appendix 2: Trade Mark / Technology Information (issue 1.0).

### 3. Short Courses

#### • **EUROSUI Granada, Spain 19/01/2005**

- **SOI Microprocessors** (Dr. Ghavam Shahidi, IBM)
- **Ultimate SOI Devices** (Prof. Sorin Cristoloveanu, IMEP)
- **SOI market and applications** (Dr. Pierre Delatte, CISSOID)
- **Partially Depleted SOI design for low power applications** (Dr. Philippe Flatresse, STMicroelectronics)
- **Simulation of SOI devices** (Prof. F. Gámiz, UGR)
- **Recent advances in SOI materials** (Dr. Bruno Ghyselen, SOITEC)
- **SOI Technology for high performance low power microprocessors** (Dr. Asanga Perera, Freescale)

Available at <http://www.eurosoi.org/tutorials.asp>

#### • **EUROSUI Grenoble, France 08/03/2006**

- **Designing Around SOI** (Dr. Bill Redman-White, Univ. Southampton & Philips)
- **Characterization and Simulation Issues for SOI Devices** (Prof. David Esseni, Univ. Udine)
- **Industrial SOI Technologies & Applications** (Dr. Piet Wessels, Philips)
- **SOI Materials Zoo (from SOS and ZMR to Unibond)** (Dr. Hubert Moriceau, LETI)
- **Multiple Gates and Strained Films for SOI MOSFETs: from Technology to Characterization and Applications** (Dr. Anne Vandooren, Freescale)
- **Non-CMOS Applications for SOI** (Prof. Neil Mitchell, Queens Univ. Belfast)

Available at <http://www.eurosoi.org/tutorials.asp>

- **EUROSUI Leuven, Belgium 24/01/2007**

- **Wideband characterization of SOI materials and devices** (Prof. J.P. Raskin)
- **Trends in SOI technologies** (Dr. O. Faynot, CEA-LETI)
- **Quantum Wire Effects in Trigate SOI MOSFETs** (Prof. J.P. Colinge, Tyndall)
- **Low-frequency Noise in SOI** (Dr. E. Simoen, IMEC)
- **SOI Materials and Process** (Dr. C. Girard, SOITEC)
- **SOI for High temperature Electronics: from Technology to Circuit Applications** (Dr. Pierre Delatte, CISSOID)

Available at <http://www.eurosoi.org/tutorials.asp>

- **EUROSUI Tyndall, Ireland 23/01/2008**

- **The SOI MOSFET: from Single Gate to Multigate** (Prof. Jean-Pierre Colinge, Tyndall)
- **Physics of the Multigate MOS System** (Prof. Bogdan Majkusiak, Warsaw University of Technology)
- **Mobility in Multigate MOSFETs** (Prof. Francisco Gamiz, University of Granada)
- **Multigate MOSFET Technology** (Dr. Malgorzata Jurczak, IMEC)
- **Radiation Effects in Advanced Single- and Multi-Gate SOI MOSFETs** (Dr. Véronique Ferlet-Cavrois, CEA)
- **Multigate MOSFET Circuit Design** (Dr. Gerhard Knoblinger, Infineon)

Available at <http://www.eurosoi.org/tutorials.asp>

- **First FDSOI tutorial of the Thematic Network on SOI technology, devices and circuits.  
Grenoble, France, 17/11/2008 - 18/11/2008.**

- **Variability Issues** (Prof. Asen Asenov, Glasgow University)
- **Fully-Depleted SOI for Nanometer Subthreshold Circuits** (D. Bol, D. Flandre, UCL)
- **Introduction of the First FDSOI Tutorial** (Olivier Faynot, CEA-LETI)
- **Compact Modeling of Undoped FDSOI MOSFET** (O. Rozeau, LETI)
- **EUROSUI+: European Platform for low-power applications on Silicon on Insulator Technology** (Prof. F. Gámiz, UGR)
- **FDSOI Devices: Physics and Characterization** (Prof. Sorin Cristoloveanu, IMEP)
- **FDSOI Circuit Design** (Alexandre Valentian)
- **FDSOI: Technology and Electrical Results** (F. Andrieu)

Available at <http://www.eurosoi.org/tutorials.asp>

- **EUROSUI Chalmers, Sweden 19/1/2009**

- **Modelling of ultra thin body SOI nano-transistors** (Prof. Luca Selmi, University of Udine)
- **Strained channel materials for SOI transistors** (Prof. Siegfried Mantl, Forschungszentrum, Jülich)
- **SOI technology: an opportunity for RF designers** (Jean-Pierre Raskin, Université Catholique de Louvain)
- **From MEMS to embedded NEMS** (Dr. Julien Arcamone, CEA-LETI, Grenoble)
- **Ultimately thin carbon on insulators: Graphene** (Dr. Max Lemme, Harvard University, Cambridge, Massachusetts)
- **SOI Circuits: Do you want Partially Depleted or Fully Depleted Devices?** (Prof. Jean-Pierre Colinge, Tyndall National Institute, Cork)
- **Digital SOI design in the nanometer era - from high-performance to ultra-low-power circuits** (David Bol, Université Catholique de Louvain)

Available at <http://www.eurosoi.org/tutorials.asp>