



Project n° IST-1-506653-CA

## **EUROSOI**

**Thematic Network on Silicon on Insulator Technology, Devices and Circuits**

**COORDINATION ACTION**

**INFORMATION SOCIETY TECHNOLOGIES**

### **D10. EUROSOI Roadmap**

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Project coordinator organisation: University of Granada, Spain

Rev.1

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<b>Dissemination Level</b>		
<b>PU</b>	Public	
<b>PP</b>	Restricted to other programme participants (including the Commission Services)	
<b>RE</b>	Restricted to a group specified by the consortium (including the Commission Services)	
<b>CO</b>	Confidential, only for members of the consortium (including the Commission Services)	X



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## **Section 1. Deliverable description**

### **Section 1.1. Introduction**

Two years ago, at the beginning of EUROSIO action at the end of 2003, Silicon on Insulator technology was already recognized by major experts, international roadmaps and semiconductor companies as the next CMOS mainstream technology, with a potential market share of 50 % of the overall Si market within the following few years. SOI was therefore already positioned as a strategic R&D field of major importance: a very promising and viable mean of improving integrated circuit performance, thus pushing the limits of CMOS technology. Our main goal in this Coordination Action is to provide the European Industry with easier access to the large amount of expertise and invaluable experience available in Europe, so that it will become the leading SOI player in the international arena. Therefore, the EUROSIO co-ordination efforts have been focused on fostering those activities which contribute to improving the role of the European semiconductor industry with regard to SOI and to the knowledge that will enable Europe to compete internationally. Different activities have been developed to reach this goal:

1. The first objective was to describe clearly where we are in Europe with regard to SOI. This leads us to the elaboration of the State-of-the-Art report (Deliverable 9). Along these two years of collaborative work we have identified the status of Silicon-on-Insulator technology in Europe, including the strong points, but also the weaknesses.
2. We have also finally identified the future challenges (short and long term) that the SOI research and industry will be facing in the following years (EUROSIO Roadmap, Deliverable 10).

To do so, we have tried to embrace a very wide study area, going from materials to technology and from devices to circuits and end-user/industrial applications. This huge task has been accomplished by means of a tight collaboration without precedent in EUROPE in the field of SOI. These documents compile the contributions of more than 150 researchers/experts from 14 European countries active in SOI technology, devices and systems. The documents have been edited by Prof. Andrés Godoy and Prof. Francisco Gámiz from the University of Granada (EUROSIO Co-ordinator).

A “Roadmap” is an extended look at the future of a chosen field of inquiry, composed of the collective knowledge of researchers in that field. The composition of a roadmap can encompass trends in the area, links and comparisons between different fields, and the identification of discontinuities or knowledge voids, and highlight potential major show-stoppers. The elaboration of this report has followed the Work Plan detailed in the Annex I of EUROSIO contract: the starting point was the conclusions and recommendations given at the end of each SoA chapter which have been used to identify the priority areas of research and formulate the strategies for the future.

During the First EUROSIO Workshop and taking into account the inputs of the partners we elaborated a first version of the Roadmap taking the SoA report as starting point. This draft version was widely discussed during the special session organized during the Workshop with this objective. The Management Board collected all the comments, suggestions and modifications and elaborated the preliminary version of EUROSIO Roadmap. This preliminary version has been extensively discussed during the second year, and especially during the Working Group meetings held in Louvan-la-



Neuve, Grenoble and Madrid in October and November 2005. We took into account the comments of our reviewers Dr. Netange (EU Commission) and Prof. Ruud Schropp (Utrecht University). The conclusions of those meetings were used to elaborate the final version of the document. The present roadmap has three different parts:

1. A short executive summary which tries to position EUROSOI with regard to the next Framework Programme of Research (FP7), ENIAC Strategic Research Agenda and 2005 ITRS document.
2. A 'Table of Challenges', where the future actions are summarized, classified in short term and long term actions.
3. And, finally the roadmap itself split in chapters, sections and subsections, following the same table of contents (TOCs) as in the State-of-the-Art report. It comprises nine (9) chapters covering a wide spectrum of the SOI activity in EUROPE according to the following table:

Partner	Roadmap Chapter
SOI Materials.	SOITEC
Devices. Characterization.	IMEP
Devices. Fabrication Technologies.	UGR
Devices. Physics.	UGR
Simulation and modelling.	UGR
Reliability.	Philips
Non-conventional devices concepts.	UGR
Circuits and systems	UCL
Industrial and End-user applications	CISSOID

Each chapter follows the structure bellow:

- A short section with comments, explaining the contents of the section.
- Strong Points and Weaknesses are identified.
- European Groups active in the field are listed.
- Finally, main recommendations and conclusions are drawn.

The SOI Roadmap is a helpful tool for European researchers since it identifies the future needs of SOI technology in EUROPE, foresees its physical limits, and provides, when possible, alternative solutions.



## Section 1.2. Workpackage description

<b>Workpackage description</b>								
<b>Workpackage number</b>	WP4	<b>Start date or starting event:</b>					6	
<b>Activity Type<sup>1</sup></b>	Coordination Activities							
<b>Participant id</b>	1	2	3	4	5	6	8	30
<b>Person-months per participant:</b>	1	1,5	1,5	1,5	1,5	1,5	1,5	1,5

### Objectives

- 1) To increase knowledge and expertise about SOI technology in Europe by enhancing interaction and synergy between academic groups and industry.
- 2) To compile, filter and provide structured information about SOI in Europe.
- 3) To foster the exchange of knowledge between research groups working in: materials, devices, circuits and electronic end-user applications.
- 4) To promote interaction between existing SOI projects at national and European level, and facilitate the coordination of their work.

### Description of work

A "Roadmap" is an extended look at the future of a chosen field of inquiry, composed of the collective knowledge of researchers in that field. The composition of a roadmap can encompass trends in the area, links and comparisons between different fields, and the identification of discontinuities or knowledge voids, and highlight potential major show-stoppers. The work directly involved the 6 WG leaders, although the experience and expertise of all partners will be very important. The workplan detailed in Section B6-a was followed by the elaboration of this report. The SOI Roadmap was updated after each MB meeting (months 18 and 27).

### Deliverables

D4. First SOI Roadmap (month 12)  
D10. Final SOI Roadmap (month 27)

### Milestones<sup>2</sup> and expected result

Identify the existing research work on SOI topics and identification of SOI strengths and weaknesses, identification of scientific priority areas, and formulation of research and development strategies.

M3. Preliminary SOI Roadmap Report. Meeting of the Management Board (month 12)

### Measures of success

- i) Customer survey
- ii) Review/report of independent experts.
- iii) Number of sold copies.

<sup>1</sup> For Coordination Actions each workpackage must relate to one (and only one) of the following three possible Activity Types: Coordination activities, Training activities, Management activities.

<sup>2</sup> Milestones are control points at which decisions are needed, for example concerning which of several technologies will be adopted as the basis for the next phase of the project.



## **Section 2. Silicon on Insulator Roadmap**

### **Section 2.1. Executive Summary**

Three organizations will determine the future of electronics in Europe in the following years: The ENIAC technological platform, the International Technology Roadmap for Semiconductors (ITRS) and the 7<sup>th</sup> Framework Programme for Research of the European Commission. The objective of this Executive Summary is to position the conclusions and recommendations of EUROSOI project with regard to these organizations.

#### **Subsection 2.1.1. EUROSOI & ENIAC**

On Page 7 of its Strategic Research Agenda (SRA) Summary, ENIAC points out five major applications for the European Industry: health, security, mobility, communication, and education. Most of SOI technology benefits will directly contribute to the successful development of these applications:

- high-speed for communication and education (higher bandwidth)
- microwave/RF for mobility, health, security (RF tags), communication and education
- ultra-low-power for health, security (tags, sensors, smart tags), communication and education
- high voltage for health, mobility, communication and education
- high temperature for mobility (transportation), and security
- radiation-hardness for health, mobility, communication and education
- MEMS/sensors integration for health, mobility, security, communication and education
- optoelectronics for health, security, communication, mobility

From a different point of view, ENIAC identifies six main research domains where it's necessary to focus work in the next years to guarantee the EU industry future:

- 1) More Moore (i.e. the continuation of scaling)
- 2) More than Moore (i.e the integration of new functions above CMOS chips)
- 3) Equipment and Materials
- 4) Heterogeneous Integration
- 5) Design Automation
- 6) Beyond CMOS

SOI technology plays a key role in at least three of these domains:

- 1) More Moore:
  - a. Thin and ultra-thin fully depleted devices.
  - b. Double-gate and multiple-gate devices are key players in the scaling down of device dimensions.
  - c. Quantum devices.
- 2) More than Moore:
  - a. SOI MEMs (accelerometers, resonators) integrated in the same chip as the electronics (SOCs).



- b. Analog/RF/microwave SOI to incorporate better passive components, isolation, analog/RF circuits, switches, in SoC solutions.
- c. Low-power and ultra-low power SOI circuits for ambient intelligence.
- d. Harsh environments SOI components in automotive, aerospace, power products.
- e. Revolutionary devices with enriched functionalities.
- f. Ultra small-volume devices enabling the smooth transition from micro to nano-electronics.

3) Equipments and Materials:

- a. Wafer bonding.
- b. Strained Silicon, Germanium-on-Insulator, Metal gate, High-K dielectrics.
- c. Bonding Engineering.

In conclusion SOI technology does have unique and significant advantages to address ENIAC requirements, and therefore it becomes a key player and indispensable tool to satisfy the ENIAC roadmap and challenges.

### **Subsection 2.1.2. EUROSOI & EU-FP7**

After the elaboration of the State-of-the-Art report (Deliverable D-9) and EUROSOI Roadmap (Deliverable D-10) we have identified the main actors, the strong points and weaknesses of Silicon-On-Insulator technology in Europe. All this information is collected in the present document, where the challenges which will have to be faced in the future are also identified.

During the running of EUROSOI network, we have corroborated that Europe:

- i. has a leading role in many fields related to SOI as a consequence of long activity in the research and development of SOI technology. (Many basic inventions were done in Europe !!);
- ii. it's a key contributor in many other fields;
- iii. but, it has a marginal position in other domains, mainly end-user and industrial applications and commercial production.

One conclusion drawn up from the present study is that this picture could change in the next years. Without a continued effort, Europe may lose its privileged situation in the SOI field threatened by the US and Asian competitors. Thus, it would be quite convenient to take appropriate measurements to avoid this to happen.

From the technological point of view, the measures and future challenges to take into consideration are collected in the present Roadmap (see section 2.2), and are in basic agreement with the issues listed in the 2005 ITRS document.

Other measures to strengthen the European Semiconductor Industry have been discussed, identified and highlighted by EUROSOI partners. Their objectives are try to be competitive, generate real economic growth and employment, and preserve the European dominant position. During these two years EUROSOI has launched different initiatives in order to fulfil these objectives.

#### What has been done to improve the previous situation?

1.- The EUROSOI workshops have become in a European forum of discussion specific to SOI where information and R&D results have been exchanged. The success of this initiative has been shown in the increasing number of participants and the quality



of the presentations. Due to this success, it has been planned a new EUROSIO workshop to be held in IMEC, Leuven, Belgium at the beginning of 2007.

2.- The EUROSIO network has improved the synergy between research centres and industry stimulating the mobility of researches (funding technical visits between them) and also through the organization of the above mentioned workshops.

3.- The promotion of courses and training activities has been a major concern of the MB. These educational activities have been focused on a wide variety of SOI-specific issues: Materials, processes, characterization techniques, devices, simulation and SOI circuits. Well known expertise in these fields have been invited as speakers and a balance between industry and academia have been also considered.

4.- Finally, one of the main outputs of this European network was the compilation of structured information to identify research priority areas and thereby to formulate research and development strategies. Deliverables 9 (SoA) and 10 (Roadmap) contain this valuable information.

The achievement of these activities has fostered the collaboration among different European centres of excellence. As an example we would like to mention the beginning of a scientific collaboration between CEA-LETI & IMEP in Grenoble and the University of Granada thanks to the technical visits promoted by EUROSIO.

However, it is necessary an extra effort to contribute to the development of end-user applications based on SOI technology, and therefore, to strengthen the position of European Semiconductor Industry.

Some actions have been taken along last years trying to solve the former lacks: MEDEA+ programs and some FP6 funded projects, as EUROSIO. However, these short-term actions have not been sufficient. For example, MEDEA+ programs granted the access to STMicro 0.13 $\mu$ m PD SOI CMOS process to participants. As a result, many more circuit developments (analog, RF and digital) have been demonstrated, what constitutes a big success. Nevertheless, MEDEA+ projects do not solve the lack in technology transfer to application often met in Europe. Recent IP projects funded by EC towards new SOI CMOS processes concentrate on materials, fabrication steps, device architectures, SRAM demonstration. They do not integrate analog/RF, or face modelling issues, or develop circuits for SoC using the new processes. With modelling starting only after process development and circuit design even later, it is not surprising that development cycles of applications are very long. Similarly, SOI circuit design has been mostly supported by MEDEA+. No FP6 EU-funded projects specifically target e.g. circuit design on very advanced CMOS processes such as IMEC's FinFETs, or CEA\_LETI's Double Gates. As a significant example of this situation we could consider the following: IMEC's 100 nm fully-depleted SOI CMOS process ended up being one of the most advanced in the world a few years ago. However, no significant circuit design has ever been attempted on such R&D processes. Their study stopped at process level, they are not maintained and hence do not serve new generations of designers.

To solve these bottlenecks and force collaboration towards product development, the SOI community, including of course the main industrial partners, from materials to processes, devices and circuits, should be gathered in a strong and tight collaborative project (NoE-like) with objectives to:

- Introduce new advanced SOI substrates (high-resistivity, ultra-thin and strained films, revolutionary materials for semiconductor film and BOX, etc).



- Involve device and circuit experts at the early stage of process development.
- Adapt models to SOI analog, RF and digital specificities and procure correct parameters to designers.
- Allow designers access to MPW fabrication with adequate design tools and component libraries.
- Design specific circuits for various products:
  - o biomedical ultra-low-power
  - o embedded processors, SRAM, EEPROM for SoC
  - o analog and RF for mixed-signal
  - o high-temperature / radiation-hardness for reliability (automotive, aerospace)
  - o embedded NEMS

The fulfilment of these objectives would be useful to validate concepts and designs, and to demonstrate them industrially. Otherwise, it will be hard to emerge with results satisfying the challenges proposed by ENIAC and this roadmap.

### **Subsection 2.1.3. EUROSOI & SOI Future Challenges.**

As can be read in the Roadmap document below there are a huge amount of challenges that have to be faced by the European industry in a near future. In this section we have tried to identify the issues that EUROSOI has identified as those where a larger impact can be obtained. They have been classified by chapters and inside them by their short or long term perspective.

#### **Chapter 1: SOI Materials**

##### *Short Term:*

- Continuous improvement of material quality
- Si-film thickness reduction to sub-10nm
- Wafer bonding schemes adapted to strained-Si and SiGe

##### *Long Term:*

- Change buried insulator for better thermal management
- Incorporate pattern below transferred layers
- Low T<sup>a</sup> wafer bonding processes
- Ge processing improvement

#### **Chapter 2: Devices: Characterization**

##### *Short Term:*

- Urgent revision of results interpretation for ultrathin SOI
- Impact of quantum confinement, strain and crystal orientation on mobility characterization.
- Extraction of thermal parameters

##### *Long Term:*

- Phonon engineering
- Use of the floating-body effects in the design of new memory devices



### **Chapter 3: Devices: Fabrication Technology**

*Short Term:*

- Metal gates with different work-functions
- High-k insulators
- Improvement of silicide source and drain structures
- Field isolation (LOCOS, MESA, Trench)

*Long Term:*

- Difficulties related with elevated source and drain
- Photonic integrated circuits

### **Chapter 4: Devices: Physics**

*Short Term:*

- High frequency devices with increased operating voltage
- Physical models for high temperature behaviour
- Optimization of SOI devices for RF applications

*Long Term:*

- Explore the possibilities of 3D integration
- Effects of new buried insulators on parameters such as breakdown voltage

### **Chapter 5: Devices: Simulation and modelling**

*Short Term:*

- Modelling of new materials, surface effects, mechanical and thermal stress
- Simulation of transport including ballistic and quantum effects
- Dynamic characteristics and HF behaviour → RF performance

*Long Term:*

- Development of a simulation tool for industrial use that includes all the steps involved in the fabrication process of a device
- Interaction between industry and research groups

### **Chapter 6: Reliability of SOI devices and circuits**

*Short Term:*

- Physics of EM process: Influence of thermal stress, materials, scaling, etc
- Study of radiation effects for aero-space applications

*Long Term:*

- ESD protection compatible with SOI devices and RF applications
- Assure the reliability of new materials for manufacturing: High-k, metal gates, strained-Si, silicides, etc.



### **Chapter 7: Physics: Non-conventional device physics**

*Short Term:*

- Thorough study of DG-SOI transistors as an alternative to conventional bulk MOSFETs (Uniform TSi<10nm, misalignment). More exploratory work for multigate transistors
- Study of the ballistic transport at different devices and materials
- Degradation of electron mobility produced by high-k materials

*Long Term:*

- Use of Schottky barriers as source and drain contacts

### **Chapter 8: Transistor modelling for circuit simulators**

*Short Term:*

- Development of compact models that includes a wide variety of effects
- Use of HR substrates for improved circuit design
- Focusing of efforts in mixed mode applications and RF design in SOI technology (telecom and automotive applications)

*Long Term:*

- Build of a complete & reliable tool to be used by industrial partners in their development efforts
- Innovative circuits and architectures

### **Chapter 9: End-user and industrial applications**

*Short Term:*

- Characterization of existing SOI processes and designed circuits under radiations
- SOI is used to make smart power chips, high-voltage drivers and high power devices. Very important for automotive and power applications
- An advanced SOI process for low-power and RF applications could offer breakthroughs for the European wireless industry

*Long Term:*

- The EC, in coordination with ESA, could support existing European SOI foundries to make their processes compatible with radiation-hard requirements

### **All these technical challenges:**

- **Agree with the ITRS-2005 but have been selected taking into account the current status of SOI technology in Europe.**
- **Are realistic (Europe capabilities) and ambitious.**
- **Identify the main objectives that have to be considered by the national and European funding agencies.**



## Section 2.2. EUROSIO Roadmap

### Subsection 2.2.1 Table of Challenges

SOI Future Challenges	Short Term	Long Term
<b>1.- SOI Materials</b>		
1.1. Commercially available substrates	<ol style="list-style-type: none"> <li>1. Continuous improvement of material quality according to ITRS Roadmap.</li> <li>2. Si-film thickness reduction to sub-10nm</li> <li>3. Cost and Yield improvements through a better control of key processes.</li> </ol>	<ol style="list-style-type: none"> <li>1. High Mobility in SOI through strained-Si and GeOI.</li> <li>2. Change buried insulator for better thermal management.</li> <li>3. Incorporate pattern below transferred layers.</li> <li>4. Low T<sup>a</sup> wafer bonding processes.</li> </ol>
1.2. Development of new SOI-like materials.	<ol style="list-style-type: none"> <li>1. Strained Si and SiGe processing.</li> <li>2. Wafer bonding schemes adapted to strained-Si and SiGe</li> <li>3. Exploration and development of crystalline orientation.</li> <li>4. Complex SOI structures.</li> </ol>	<ol style="list-style-type: none"> <li>1. Ge processing improvement.</li> </ol>
1.3. Material Characterization	<ol style="list-style-type: none"> <li>1. Assesment of viability of 450mm wafers.</li> <li>2. Solve urgent issues related to characterization of sub-10nm thick films: models needed.</li> </ol>	<ol style="list-style-type: none"> <li>1. Develop contactless electrical characterization by extending pseudo-MOSFET concepts.</li> <li>2. Develop techniques for measuring the thermal conductivity.</li> </ol>
<b>2.- Devices. Characterization</b>		
2.1. C-V measurements	<ol style="list-style-type: none"> <li>1. Refinements for ultrathin SOI films and non-standard SOI.</li> </ol>	
2.2. Lifetime characterization.	<ol style="list-style-type: none"> <li>1. Urgent revision of results interpretation for ultrathin SOI.</li> </ol>	
2.3. MOSFETs parameters extraction techniques	<ol style="list-style-type: none"> <li>1. Development of software tools to extract parameters for the most advanced models.</li> </ol>	<ol style="list-style-type: none"> <li>1. European SOI characterization network needed.</li> </ol>
2.4. Transport measurements	<ol style="list-style-type: none"> <li>1. Accurate mobility characterization in sub-10nm.</li> <li>2. Impact of quantum confinement.</li> <li>3. Impact of strain.</li> <li>4. Impact of crystal orientation.</li> </ol>	
2.5. Phonons in SOI	<ol style="list-style-type: none"> <li>1. Determination of thermal behaviour of SOI structures.</li> </ol>	<ol style="list-style-type: none"> <li>1. Phonon engineering.</li> </ol>
2.6. Charge pumping	<ol style="list-style-type: none"> <li>1. Application to sub.10nm thick films.</li> </ol>	
2.7. Electro-luminiscence techniques	<ol style="list-style-type: none"> <li>1. Assessment of emission mechanisms at low voltages and SOI structures.</li> <li>2. Development of sensitive detectors for energies below 1eV.</li> </ol>	
2.8. Noise and fluctuations	<ol style="list-style-type: none"> <li>1. New developments in connection to the noise spectroscopy are needed in particular improvements in the following areas: extra thin SOI films, tunnelling gate oxides, quantum related transport.</li> </ol>	
2.9. Transient and history effects	<ol style="list-style-type: none"> <li>1. Study of transient and history effects in single-gate and multiple-gates fully depleted technologies.</li> </ol>	



2.10. Floating body effects	1. Development of techniques related to the dynamic characterization of floating body effects.	1. Use the recently discovered floating-body effects for conceiving new types of memory devices.
2.11. Ultrathin film effects	1. Experimental characterization of ultra thin film effects in MOSFETs and quantum related effects must be increased in Europe, as experimental transistors are now available with SOI layer thinner than 10nm.	
2.12. Self Heating	1. Extraction of thermal parameters. Development of new insulator materials.	
2.13. Multiple gate devices	1. Development of new characterization tools.	1. Apply 3D gate coupling effects to develop new schemes of circuit operation.
2.14. SOI high voltage transistors	1. Compact formulation of models and development of advance simulation techniques.	
<b>3.- Devices. Fabrication Technology</b>		
3.1. SOI CMOS Technology	<b>Field Isolation:</b> 1. LOCOS: bird's beak and high tensile nitride stress that can generate dislocations in the silicon. 2. MESA ISOLATION: gate over-etching, gate dielectric integrity at mesa sharp corners and sidewall parasitics 3. TRENCH ISOLATION: TI strain-induced device degradation, micro-scratches and gouges and control of over and under polish.	
	<b>Channel and mobility engineering:</b> 1. Quality improvement of strained-Si silicon layers that can be worse than the conventional ones. 2. Processing issues specific to the strained Si and Ge, or C, containing material, will need to be addressed: a. Ultra-thin (1 nm) gate oxides, effects of strain and Ge content on oxidation rate and reducing gate leakage b. Laser doping for ultra shallow junctions, lateral channel profiling c. Device isolation: STI, self aligned STI d. Smart-cut and wafer bonding processes for SSOI 3. More work still necessary in the characterization and simulation of these devices: a. Material and device characterisation are crucial to understanding, and vital for making progress. b. New scattering models have to be developed	1. These devices must be incorporated into standard CMOS production. However, within Europe there is considerable experience of putting research material through standard process lines and developing new process modules



	<b>Source and drain engineering:</b> 1. Improvement of silicide source and drain structures	1. Elevated source and drain difficulties to be addressed: <ol style="list-style-type: none"> <li>a. Voids formation during silicidation.</li> <li>b. Increased SD junction resistance when the silicide thickness reaches the silicon film thickness.</li> <li>c. Very thin Si films are quasi-stable: agglomerate into silicon islands.</li> </ol>
3.1. SOI CMOS Technology (cont.)	<b>Gate engineering:</b> 1. Gate dielectric reliability; 2. Metal gates: Eliminates boron penetration. 3. Phase uniformity of the NiSi throughout the structure. 4. Local silicidation rate that can vary highly depending on nucleation conditions.	
3.2. High voltage devices	1. Strengthen academic research in SOI-LDMOS processes for automotive electronics and audio amplifiers.	1. SOI-BiCMOS integration. 2. Systems-on-a-chip solutions need efficient isolation of the different circuits blocks. 3. Greater engagement with Industry.
3.3. RF and Power devices	1. Fabrication of HBT devices on thin film substrates.	1. Demonstration of RF-power SOI-LDMOS integrated with CMOS.
3.4. Optical SOI technology	1. Strengthen academic research through co-ordinated and integrated projects.	1. Major platform for photonic integrated circuits. 2. Cost-reduction strategies. 3. Optimization of single UV-lithographic step.
<b>4.- Devices. Physics</b>		
4.1. Classical SOI MOSFETs	1. Special adjustments to standard transport models, like hydrodynamic or six-moments models, used in numerical device simulators, are required in order to address correctly the floating body effect in PD-SOI. 2. Extremely tight tolerance with respect to parameter variations, like Si thickness and oxide thickness fluctuations, gate length, gates alignment, etc. are the most serious technological problems, which has to be solved to support the ultimate success of ultra-thin body SOI MOSFETs.	1. Vast potential of SOI MOSFETs in accumulation mode for conventional and advanced applications, like single-electron room temperature operation or quaternary logics, is yet to be revealed.
4.2. High Voltage and Power devices	1. Renew European research effort dedicated to power devices for new SOI substrates. 2. Reduced device breakdown voltage in scaled technologies. 3. High-frequency devices with increased operating voltage for base station applications.	1. The success of future Ambient Intelligence technologies is directly attached to the improvement of power switches on SOI.



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4.3. RF devices	<ol style="list-style-type: none"> <li>1. Minimisation of collector resistance as a key issue in SiGe HBTs on SOI.</li> <li>2. Further improvement of SOI base material for bipolar properties (high minority carrier lifetime).</li> <li>3. Development of high-performance and low-cost RF and analog/mixed-signal solutions.</li> <li>4. Improvement of signal isolation.</li> <li>5. Optimizing RF/analog CMOS and SOI devices with scaled technologies: mismatch, <math>1/f</math> noise, and leakage with high-k gate dielectrics.</li> <li>6. High density integrated passive element scaling and use of new materials: Q-factor value for inductors; matching and linearity for capacitors.</li> <li>7. Reduced power supply voltages: degradation in SNR (signal-to-noise ratio) and signal distortion performance.</li> <li>8. Compound semiconductor substrates with good thermal dissipation and process equipment for fabrication at low cost.</li> </ol>	1.- Industry involvement.
4.4. SOI MEMs and NEMs	<ol style="list-style-type: none"> <li>1. Strengthen academic research through co-ordinated and integrated projects.</li> </ol>	1. Reliability issues.
4.5. Optical SOI-Waveguides		<ol style="list-style-type: none"> <li>1. Cost reduction strategies necessary to make the concept development viable.</li> </ol>
4.6. 3-Dimensional Integration		<ol style="list-style-type: none"> <li>1. Huge challenge for designers.</li> <li>2. More efforts should be dedicated to explore the possibilities of 3D integration.</li> </ol>
4.7 Novel devices	<ol style="list-style-type: none"> <li>1. Resonant tunneling in the SiO<sub>2</sub>/Si/SiO<sub>2</sub> system needs more experimental confirmation.</li> <li>2. Verify if concepts imported from III-V devices can be accommodated in SOI.</li> </ol>	<ol style="list-style-type: none"> <li>1. Resonant tunneling in the SiO<sub>2</sub>/Si/SiO<sub>2</sub> structures should be one of the strategic topics for the European nanoelectronics R&amp;D groups, both in theory and technology.</li> <li>2. More collaboration between theoretical - simulation groups and industrial partners with a ultrathin double gate SOI technology is highly recommended.</li> </ol>
4.8 Operation at high temperatures	<ol style="list-style-type: none"> <li>1. Development of physical models for high temperature behaviour.</li> <li>2. Development of circuit models (C-continuous) for high temperature operated AM SOI pMOSFETs for long and short channels is necessary.</li> </ol>	<ol style="list-style-type: none"> <li>1. Study of the effects of new buried oxides (Si<sub>3</sub>N<sub>4</sub>) and optimization of device parameters such as breakdown voltage.</li> </ol>



**5.- Devices. Simulation and modelling.**

<p>5.1. Process simulation</p>	<ol style="list-style-type: none"> <li>1. Important points concerning Algorithms: Need for robust, reliable 3D grid generation especially for process simulation, faster linear solvers, and exploit parallel computation.</li> <li>2. The following issues have to be taken into account in order to improve the models and the accuracy of the simulations:             <ol style="list-style-type: none"> <li>a. High-k dielectrics and gate materials (material properties, interfaces, impurity diffusion).</li> <li>b. Ultra-shallow junction formation, which starts from very low energy implant and especially focuses on the thermal annealing and diffusion of dopants.</li> <li>c. Enhancement of models for Si based materials, including stress/strain and including flash/laser anneals and solid phase epitaxy.</li> </ol> </li> <li>3. Topography modeling (deposition homogeneity).</li> <li>4. Planarization (cell-level CMP chip-level including dummy placement optimization, padwear and conditioning disc modeling, physics-based optimizations of rates, uniformity, and defect reduction).</li> <li>5. Surfaces (physics based feature scale models, integration of feature-scale simulation with equipment).</li> <li>6. Plasma models.</li> <li>7. The modeling of stress and strain and their influence on diffusion and activation has become vital, especially for strained silicon, SiGe, and SOI structures.</li> </ol>	<ol style="list-style-type: none"> <li>1. Co-ordination efforts important to build a reliable and complete tool for industrial use.</li> </ol>
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<p>5.2. Device simulation</p>	<ol style="list-style-type: none"> <li>1. Thermal-mechanical modeling: Need for thermo-mechanical-integrated models, include SOI properties.</li> <li>2. Important points concerning Algorithms: Need for robust, reliable 3D grid generation especially for process simulation, faster linear solvers, exploit parallel computation.</li> <li>3. Interfacial effects (plasma excitations, optical phonons, surface roughness, confinement) play the major role in determining the performance of decananometric devices.</li> <li>4. Accurate predictive models for new materials (strained silicon, germanium, gate stacks including high-k) should be further pursued.</li> <li>5. Ballistic transistors should be the subject of primary attention in the next few years. Most of devices fulfilling the ITRS predictions by the year 2007 should present quasi-ballistic transport features.</li> <li>6. Increase cross-discipline efforts will be vital in order to leverage on the expertise of fields that were originally not related and are now needed to work together to cope with the challenges outlined in this document.</li> <li>7. Identify more in detail in which way simulation can most efficiently support the industrial development. Interactions between industry and research groups must continue to be enhanced and extended. This interaction must also include the promotion and enabling of mid- to long-term research actions needed in modeling and simulation.</li> </ol>	<ol style="list-style-type: none"> <li>1. So far the efforts have been mainly devoted to modelling the static device characteristics (e.g. mobility and drain current). The aspects related to the RF performances, and in particular the comparison between the different device architecture are still at a preliminary status.</li> <li>2. Accurate modelling of high-frequency noise is one of the critical issues to guarantee the success of future nanoscale SOI transistors.</li> <li>3. Ensemble Monte Carlo simulation of Partially-Depleted SOI transistors is still an open field. In this case, together with the previously mentioned know-how about the calculation of dynamic and noise parameters, a bipolar simulation is required in order to take into account the contribution of the substrate (majority carriers) to the high-frequency performance of the transistor.</li> <li>4. Quantum-based and non-equilibrium (ballistic) device simulations are needed. Simulations must also be applicable to non conventional SOI devices (Finfets, GAA, Trigates, etc). Stress engineering must be enabled. Besides accuracy, efficiency is a key issue.</li> <li>5. Identify more in detail in which way simulation can most efficiently support the industrial development.</li> </ol>
<b>6.- Reliability of SOI devices and circuits</b>		
<p>6.1. Wafer Level Reliability</p>	<ol style="list-style-type: none"> <li>1. SOI unique defects, which lead to time dependent failures, have to be minimized to acceptable levels.</li> <li>2. Additional work on clean processing and improved gettering techniques would be useful.</li> <li>3. The following measures should be considered when characterizing the wafer-level reliability: Defect density (&lt;0.1 defects/cm<sup>2</sup>) across wafer, wafer-to-wafer, and lot-to-lot.</li> <li>4. Intra-wafer and inter-wafer variations produced by chemical-mechanical polishing (CMP) need consideration on all material properties.</li> </ol>	<ol style="list-style-type: none"> <li>1. A further integration of European activities in terms of contaminant control and characterization methods through joint projects is necessary.</li> <li>2. A division of tasks between universities (mid- and long-term research, characterization methods) and industry (application-oriented improvement methodologies) is recommended.</li> </ol>



<p>6.2. Electro static discharge (ESD)</p>	<ol style="list-style-type: none"> <li>1. High current ESD device models compatible with running on industry standard spice simulators with self-heating and breakdown models incorporated into the compact equivalent circuit.</li> </ol>	<ol style="list-style-type: none"> <li>1. Most protection schemes developed for bulk may not be compatible with SOI structures. Develop a new set of ESD protection algorithms and circuits as conventional (bulk) ESD designs cannot be copied over to SOI (much SOI-specific design is necessary).</li> <li>2. RF quality ESD device models for RF applications (diodes, silicided and nonsilicided MOSFETS).</li> </ol>
<p>6.3. Latch-up</p>	<ol style="list-style-type: none"> <li>1. Development of latchup device simulators with improved convergence and with breakdown and temperature models turned on.</li> <li>2. Design of effective guarding designs in I/O circuits.</li> <li>3. Reduced NWELL and PWELL sheet resistances for improvements in trigger currents while minimizing junction area capacitances and maintaining low junction area leakages for low power applications.</li> <li>4. Increased shallow trench isolation (STI) depths for reduction in parasitic betas.</li> </ol>	<ol style="list-style-type: none"> <li>1. Development of RF quality parasitic NPN and PNP models for accurate transient latchup simulations.</li> <li>2. Improved extraction tools/algorithms to extract only the most important parasitic latchup structures.</li> </ol>
<p>6.4. Electro-migration</p>	<ol style="list-style-type: none"> <li>1. This topic provides a new challenge for thermal and mechanical device simulators, which is currently not well covered. Electromigration should have priority on those tools that simulate failure mechanisms. Topics to be considered:             <ol style="list-style-type: none"> <li>a. Physics of mass transport and EM: diffusion mechanism (surface, lattice, grain boundary diffusion), current and temperature dependence, controlling a dominant diffusion mechanism (failure mode).</li> <li>b. Different resistance change vs. time characteristics under EM or thermal stress: spikes, gradual increase, abrupt failures during aging.</li> <li>c. Scaling of EM to smaller line sizes.</li> <li>d. Effect of ambient gases during EM testing (e.g., air vs. nitrogen).</li> <li>e. Interaction between EM and stress migration.</li> </ol> </li> </ol>	



6.5 Radiation effects	<ol style="list-style-type: none"> <li>1. This field could be crucial for the newly extended space activity of the European Union. Reliance on US technology could be detrimental for independent defense projects.</li> <li>2. Confirm that standard FinFET devices are intrinsically radiation-hard. This is a very strong argument for developing this technology.</li> </ol>	
6.6. Mechanical effects: Strain and thermal cycling	<ol style="list-style-type: none"> <li>1. It is necessary a deeper knowledge of thermo-mechanical stress effects.</li> </ol>	<ol style="list-style-type: none"> <li>1. The area of mechanical fatigue on a micro-mechanical scale is poorly understood and will require further studies. Extensive work on this reliability issue is needed in terms of understanding and prevention of catastrophic failures.</li> </ol>
6.7 Application Specific Tests	<ol style="list-style-type: none"> <li>1. There is currently no European effort to develop application-specific tests to understand and model the reliability of SOI devices.</li> </ol>	
6.8 Novel Materials. Novel failure mechanisms	<ol style="list-style-type: none"> <li>1. Coordination with work going on in bulk materials.</li> </ol>	<ol style="list-style-type: none"> <li>2. Multiple material changes are projected by 2008 or so (high-k gate dielectric, metal gate electrodes, strained Si, nickel silicide, etc). Near mid-gap metal gate electrodes will be desirable to set the threshold voltage for UTB SOI. Assuring the reliability and implementing into manufacturing all these new materials, processes, and structural changes in a relatively short period of time will be a difficult challenge.</li> <li>3. Establish network to pay attention to SOI-specific reability requirements and challenges.</li> <li>4. Extensive collaboration between research centres (universities: modelling and understanding) and industry (providing critical statistical information) is recommended and requires some coordination.</li> <li>5. Integration of some leading MEMS players in this field is strongly recommended.</li> </ol>
<b>7.- Physics. Non-conventional device physics</b>		
7.1. Transport Enhacement FETs	<ol style="list-style-type: none"> <li>1. Study of the impact of quantum effects in UTB MOSFETs with body thickness under 10 nm.</li> <li>2. Control of boron penetration from doped polysilicon gate electrode.</li> <li>3. Control of silicon loss at spacer etch and gate etch needs to be much tighter on thin SOI and SiGe wafers, where the total silicon thickness is 20-50 nm.</li> <li>4. Minimized depletion of dual-doped polysilicon electrodes.</li> </ol>	<ol style="list-style-type: none"> <li>1. Increased funding of long term research. Only SOI can extend the Moore's law and guarantee the soft transition from micro to nano-electronics.</li> <li>2. Identifying, selecting, and implementing novel interconnect schemes.</li> </ol>



7.2. Metallic gate FETs	<ol style="list-style-type: none"> <li>1. The use of metal gates will be mandatory to overcome poly-Si drawbacks.</li> <li>2. Much experimental work should be done in this topic since different questions remain unsolved (e.g.: Metal gate still suffer from the inadequate tuning of the workfunctions for threshold voltage (<math>V_{th}</math>) definition of both n- and p-MOS.</li> </ol>	
7.3. Ultrathin body SOI FETs	<ol style="list-style-type: none"> <li>1. Exploring intensively several fabrication issues related with the control of the threshold voltage and silicon body thickness and defect density.</li> <li>2. Other major issue is the impact of quantum effects in UTB MOSFETs with body thickness under 10 nm.</li> </ol>	<ol style="list-style-type: none"> <li>1. Influence of confined phonons on transport properties.</li> </ol>
7.4. Source and Drain Engineering	<ol style="list-style-type: none"> <li>1. At the present moment this technology is still under development, so still more research at the academic and industrial level is needed in the short and mid terms to make it completely feasible for commercial applications.</li> </ol>	<ol style="list-style-type: none"> <li>1. Strong efforts must be made to determine the possibilities of SB-MOSFETs for analog high-frequency applications.</li> </ol>
7.5. Double Gate Devices	<ol style="list-style-type: none"> <li>1. European groups are strong in the field of theory and simulation of the double gate SOI devices as well as there is knowledge and practical experience for implementation of this technology into the industry.</li> <li>2. Misalignment of gates is an important technological challenge since it produces a degradation of device performance.</li> </ol>	<ol style="list-style-type: none"> <li>1. Tighter collaboration between universities and industry is strongly recommended in order to check simulators and models with experimental data.</li> </ol>
7.6. Multigate Devices	<ol style="list-style-type: none"> <li>1. One of the major challenges related with the fabrication of FinFETs is that the fins need to be a fraction (<math>\frac{1}{3}</math>-<math>\frac{1}{2}</math>) of the gate length thus requiring sub-lithographic techniques.</li> <li>2. Minimized depletion of dual-doped polysilicon electrodes.</li> </ol>	<ol style="list-style-type: none"> <li>1. Exploratory work to understand vertical transistors, Trigate and Gate-all-around devices.</li> <li>2. The potential of these devices for conceiving new circuit functionalities should be systematically explored.</li> </ol>
7.7. Ballistic transistors	<ol style="list-style-type: none"> <li>1. Understanding of this phenomenon by the use of physical models, device simulations and if possible actual fabrication of devices.</li> <li>2. The present gap between the results predicted by analytical models and rigorous simulations has to be bridged. Study of the issues that impede the ballistic transport, like reducing the channel scattering, improving the Si-SiO<sub>2</sub> interface and use of multiple gate structures.</li> </ol>	<ol style="list-style-type: none"> <li>1. The use of different channel materials (strained-silicon or germanium), featuring higher injection velocity and lower scattering, is expected to enhance the on-current.</li> </ol>
7.8 High-k materials	<ol style="list-style-type: none"> <li>1. Removal of high-k dielectric without loss of the underlying silicon, especially in the case of SOI or non planar devices.</li> <li>2. Exploratory work to understand the degradation of the electron mobility produced by remote polar-optical phonons.</li> </ol>	<ol style="list-style-type: none"> <li>1. Metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization.</li> </ol>

8.- Transistor modelling for circuit simulators		
8.1. Transistor modelling for circuits simulators	<ol style="list-style-type: none"> <li>1. Points that need to be addressed by future compact models are:               <ol style="list-style-type: none"> <li>a. Proper modeling of series resistances in active devices.</li> <li>b. Non-quasi-static models.</li> <li>c. Influences of statistic aspects on device parameters.</li> <li>d. Quasi-ballistic effects, to be analyzed and addressed in strict cooperation with device modeling groups.</li> <li>e. Concerning interconnects and integrated passives: Need for on-chip inductance effects, frequency dependent resistance, hierarchical full chip RLC, inclusion of reliability aspects.</li> </ol> </li> </ol>	<ol style="list-style-type: none"> <li>1. European coordination of the know-how, and most important the possibility to build a complete and reliable tool to be used by industrial partners in their development efforts would be very desirable.</li> </ol>
8.2. Digital Logic	<p><b>High-speed:</b></p> <ol style="list-style-type: none"> <li>1. It is highly desirable to grow and exploit it in SoC mixed-signal design, where general purpose and dedicated processors are integrated with analog and RF, targeting wireless telecommunications where EU holds an outstanding position.</li> </ol>	<ol style="list-style-type: none"> <li>1. EU researchers should contribute to demonstrate the performance of advanced and alternative technologies (e.g. double gate, finfet, multiple-gate SOI MOSFETs) on basic digital circuits for high-speed applications.</li> <li>2. A new paradigm for CMOS circuits taking advantage of multiple-gate inputs should be developed.</li> </ol>
	<p><b>Low-power/Low voltage:</b></p> <ol style="list-style-type: none"> <li>1. (Multi-Threshold CMOS techniques are still difficult to implement in deep-submicron technologies because only 1 or 2 threshold voltage values are available, which is not enough in some digital designs, especially in designs that require a negative <math>V_T</math> for n-type and p-type transistor.</li> </ol>	<ol style="list-style-type: none"> <li>1. Some open issues such as noise immunity, delay penalty compensation based on innovative circuits and architectures need to be addressed by the research community in Europe.</li> </ol>
8.3 Memories	<ol style="list-style-type: none"> <li>1. It is fundamental to have at disposal memory generators (all views, from layout to HDL) and reliable models for design and simulation. This is a key point that the circuit design research community in the SOI field should pursue so as to facilitate the successful adoption of this technology by the EU industry.</li> <li>2. NVM (EEPROM) should be developed and offered on SOI to broaden application scope of mixed-signal products.</li> </ol>	<ol style="list-style-type: none"> <li>1. Develop capacitance-less DRAMs based on new floating-body effects.</li> </ol>



<p>8.4. Analog and RF</p>	<ol style="list-style-type: none"> <li>1. There are not many European groups working on the compact modeling of SOI MOSFETs in RF.</li> <li>2. Although analogue circuit design is a tough and challenging task, it will never drive the markets. So, processes targeting mixed-mode applications, allowing the integration of digital circuitry and embedded memories will make the decision. Analogue design will follow.</li> <li>3. SOITEC work has resulted in commercial large-diameter HR substrates with effective resistivity of 200 Ohm-cm. Therefore, from the material side, SOITEC is waiting for device guys a signal to invest for mass production.</li> <li>4. Extend to RF the multiple-gate SOI MOSFETs models recently developed by several European groups.</li> <li>5. Europe should focus their efforts in mixed mode applications and also on RF design in SOI technology with emphasis on telecom applications and automotive.</li> </ol>	<ol style="list-style-type: none"> <li>1. Demonstration of RF SOI circuits.</li> <li>2. In a near future, higher resistivity substrate (<math>&gt; 1000 \text{ Ohm}\cdot\text{cm}</math>) demonstrated in EU labs on small diameter wafers and with only passive microwave test structures should be transferred to large-diameter CMOS platforms.</li> </ol>
<p><b>9. End-user and industrial applications</b></p>		
<p>9.1. Radiation hard products</p>	<ol style="list-style-type: none"> <li>1. Characterization of existing SOI processes and designed circuits under radiations.</li> <li>2. Guaranty the durability of existing SOI processes in Europe (X-Fab, ST).</li> </ol>	<ol style="list-style-type: none"> <li>1. The EC, in coordination with ESA, could support existing European SOI foundries to make their processes compatible with radiation-hard requirements.</li> </ol>
<p>9.2. High temperature products</p>	<ol style="list-style-type: none"> <li>1. Research on wide-gap materials on Insulators (GaN, SiC) could be useful for high-temperature application</li> </ol>	<ol style="list-style-type: none"> <li>1. High-temperature Electronics based on SOI could become strategic for the European industry (Oil &amp; Gas, Aeronautic &amp; Space but also Automotive). SOI high-temperature electronics bases exist in Europe but the industrialization is still weak and should be improved through R&amp;D projects or supporting companies active in this field.</li> </ol>
<p>9.3. High-speed products</p>	<ol style="list-style-type: none"> <li>1. SOI microprocessors applications are dominated by US Companies, having some activities in Europe. This is probably not the field were Europe has to compete. However, Europe has not to leave advanced SOI technologies to foreign companies because SOI will bring huge benefits for low-power and RF applications were European companies are key players.</li> </ol>	



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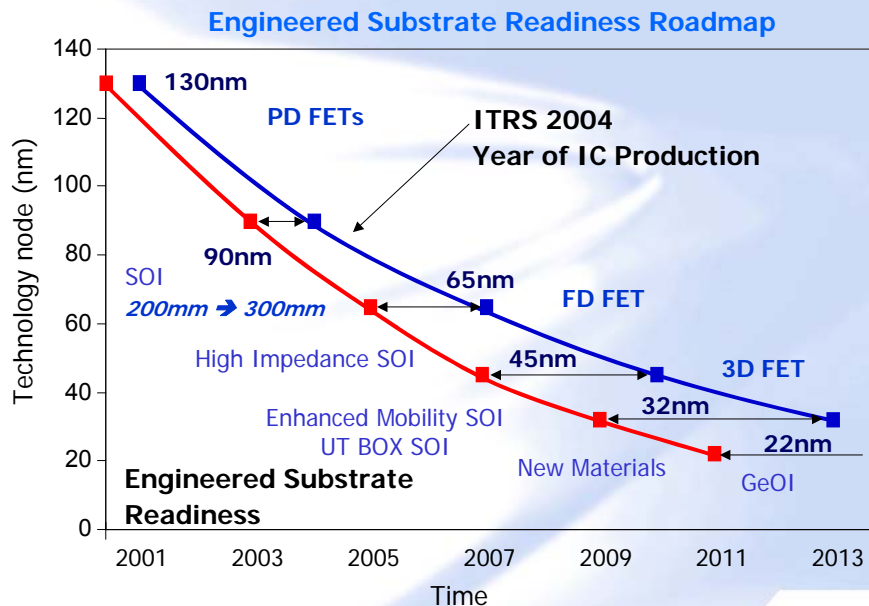
9.4 High-voltage products	<ol style="list-style-type: none"> <li>1. SOI is used to make smart power chips (automotive, Audio), high-voltage drivers but also high power devices.</li> <li>2. This is very important for the automotive and power semiconductor applications, both markets where Europe has a strong position.</li> </ol>	
9.5. Ultra-low voltage & Low-power products	<ol style="list-style-type: none"> <li>1. A low-power SOI process available through a Multi-Project-Wafer (MPW) available in Europe should be of great interest.</li> </ol>	
9.6. Microwave & RF Products (Wireless applications)	<ol style="list-style-type: none"> <li>1. An advanced SOI process for low-power and RF applications could offer breakthroughs for the European wireless industry.</li> <li>2. Open existing processes for MPW access and industrialization could produce new ideas and applications to emerge.</li> <li>3. Capitalizing on the results and experience already obtained in Medea+ T206 project to address and develop more advanced processes, following both the "more More" (next technology nodes) and "more than More" (adding process options on existing processes) strategies.</li> </ol>	

## Section 2.2.2 EUROSOI Roadmap

### CHAPTER I. SOI Materials

#### Comments

Departing from standard commercially available SOI substrates, new generations of SOI materials and other so-called engineered substrates will have to be developed. The figure hereafter is an attempt to give an overview of which CMOS nodes are targeted, and therefore when such new generations of substrates will have to be delivered. This graph contains two quasi parallel plots to illustrate that the developments on the material side always have to anticipate by a few years the needs coming from device developments.





### 1.1.- Commercially available SOI substrates and key manufacturing steps.

#### Comments

During last decades, several techniques have been developed with different levels of success for the realization of SOI substrates. The table here below lists most of them, with an effort to review their compatibility with large volume/high quality compatibility as well as full and homogeneous wafer treatment.

Approach family	Technique	Full wafer capability (or islands only)	Industrial mainstream ?
<b>Epitaxy</b> (including Hetero epitaxy and Solid Phase Epitaxy)	SOS etc ...: Silicon On Sapphire	Y	+
	ZMR : Zone Melting Recrystallization	Y	0
	ELO : Epitaxial Layer Overgrowth	Y	0
	Others		
<b>Substrate / layer transformation</b>	DI : Dielectric isolation	N	0
	FIPOS : Full Isolation by Porous Oxidised Silicon	N	0
	SIMOX	Y	.+++
	SON	N	***
	Others		
<b>Wafer bonding / layer transfer</b>	BSOI, BESOI	Y	.+++ (thick SOI)
	ELTRAN	Y	.+++
	Smart Cut (Unibond)	Y	.+++
	Others		

It appears that only a few of them are really used today to (or have the potential to) produce commercially large volume quantities of SOI materials with appropriate quality. Mainly two families of techniques are really emerging : SIMOX and wafer bonding techniques (BSOI, Smart Cut, ELTRAN). Some other more marginal but existing technologies such as SOS (Silicon On Sapphire) and SON (Silicon On Nothing) still show some potential for some specific applications.

#### European position on the field

Europe is very well positioned today and even leader in the field of wafer bonding based techniques, especially with the Smart Cut process (SOITEC technology, licensed in addition to WACKER–Siltronic) and several medium-small size companies (or medium-small size divisions of larger companies) involved in BESOI like techniques. One specific technology within this family, ELTRAN, is clearly dominated by Japan with CANON.

Europe is almost totally absent in the field of SIMOX technologies.

The table here below shows who are the main actors in Europe and on which technology they are present (and leading most of the time). It can be seen that not only European material suppliers but also European specific equipment suppliers and public R&D institutions are present and leading.

This pictures clearly shows the strength of Europe in wafer bonding at every level.



Technique	Approach family	SOI Material supplier	Specific Equipment Supplier	R&D Labs
SIMOX	Substrate / layer transformation	?	High Dose Ox implanters : None	?
BSOI, BESOI	Wafer bonding / layer transfer	Okmetic, Umicore, Tracit, ...	Wafer bonding machines: EVG, Karl-Zuss	LETI MPI-Halle VTT QUB Chalmers, etc ....
ELTRAN		None		
Smart Cut (Unibond)		SOITEC, SILTRONIC		

Overall, although Europe has been pioneering in the field, the situation today is that many actors have entered into the arena, and have engaged significant resources. As a result, especially on the Intellectual Property side, many application patents (more or less sensible) have been filed on many topics related to such a technology. Europe's leading position here is threatened.

### Technical challenges

Concerning the technical challenges, on the short term they are addressing:

- Continuous improvement of material quality in line with the industry roadmaps (ITRS etc ...).
- Thickness reductions towards sub-10nm dimensions and a strong focus on thickness uniformities at large diameter wafer scales.
- Technology cost and technology yield improvements through a better control of each of the key steps of the technology (wafer bonding, splitting, finishing steps).

On the longer term, many other key developments do exist to build the next generations of SOI wafers and concern for instance: high mobility in SOI thanks to strained-Si or Ge On Insulator and others, changing the buried insulator for better thermal management purposes, incorporating patterns into or below the transferred layers.

Other developments will consist in adapting the SOI wafers for some specific applications (which do not rule out high volume). For instance, RF applications require high resistivity substrates. Wafer bonding techniques, among which Smart Cut, enable specific solutions consisting in reporting high quality transistor grade silicon film onto high resistivity silicon. Other specific substrates may concern high power devices, MEMS, Opto devices, etc.

Usually a wafer bonding preparation based on wet chemistry pre-cleaning is associated with a post-bonding high temperature annealing (>1000°C) to transform low/medium bonding energy into a strong covalent one. The wafer contacting and bonding step is usually performed at room temperature. While lower energies can be tolerated for some applications, SOI wafer processing in general can not afford it. For future evolutions of SOI materials, there is a need to go to high bonding energies, using processes without the use of high temperature anneals: the so-called Low T<sup>a</sup> wafer bonding processes (Low T<sup>a</sup> refers to the maximum temperature used in the post bonding annealing).

Most of the European labs involved in wafer bonding have also high energy bonding programs. However, in the field of low T<sup>a</sup> wafer bonding, Europe today does not have a dominant position, with strong contributions in the US and Japan. Low T<sup>o</sup> wafer bonding is one topic of the future and should be addressed carefully, for instance by gathering together the many rich but elementary activities spread across Europe.



### **Strong Points**

- Leadership on wafer bonding science and technology  
(MPI-Halle, CEA-LETI, SOITEC, EVG, Karl-Zuss, QUB, VTT, Okmetic, Chalmers , ...)
- Leadership on wafer bonding tools  
(EVG, Karl-Zuss)
- Leadership based on the Smart Cut process (SOITEC, CEA-LETI) for industrial exploitation  
(MPI-Halle, CEA-LETI, VTT) for basic research
- Competitive contributors in BSOI / BESOI (Tracit, UMICORE, Okmetic )
- Leadership in SON (ST)

### **Weak Points**

- Aggressive competition outside Europe (US and Asia).
- Very small activity in other approaches than wafer bonding + Smart Cut.
- No (or almost no) activity in SIMOX, Porous silicon splitting or SOS where the activities are developed in Asia and US. Leading activities in combination of wafer bonding and porous layer splitting in Asia (Canon). Strong contributions on combination of plasma bonding and Smart Cut alike techniques in the US (SiGen). Strong contributions on wafer bonding in the US (NRL, EVG) and Asia (Tokyo)

### **Conclusions and recommendations**

- Almost no SIMOX material activity in Europe: Closing the gap would be too expensive and SIMOX is not the present European solution.
- European overall leadership in wafer bonding science and technology.
- Importance of wafer bonding technologies for most of the techniques available in Europe.
- Thin SOI market potential much bigger than thick SOI due to the perfect match with future mainstream CMOS needs.
- European leadership in thin SOI material market with Smart Cut.
- European activities well behind international efforts in some combinations of wafer bonding and wafer splitting/thinning techniques.
- A further integration of European activities through joint projects necessary.
- Focus resources on keeping leadership on wafer bonding, Smart Cut and thin SOI material market to keep pace with US and Asia in terms of innovation, IP.

### **1.2.- New SOI-like materials in development**

The potential of developments on the SOI material side is huge. Beyond simple evolutions (like quality improvement, thickness reductions towards nanometric dimensions, ..), it is envisioned that the starting substrate incorporates in the future more and more added value to bring enabling solutions at the device level.

#### **1.2.1 High mobility SOI substrates**

##### **Comments**

One of the hottest and more strategic R&D topics today is about improving carrier mobilities. Improving the carrier mobility, in addition to adopting SOI architectures, is becoming a priority if one wants to meet the next challenges raised by the ITRS roadmap for the sub 65nm nodes (drive current, ION/IOFF trade-off, ...). Strained Si in a "local strain" configuration is already implemented by several actors for the 90nm node, on bulk SI as well as on standard SOI. As a next step to further boost carrier



mobilities and device performance, combining biaxial global strained Si, uniaxial local strain and SOI will more precisely address 65nm and below nodes, depending on the applications. High performance devices (logic applications, ..) will be the first to benefit from / require such evolutions

Several families of solutions have the potential to be implemented at the substrate level, especially in combination of wafer bonding technologies which are the European strong points. Among those solutions are

- Crystalline orientation effect and hybrid orientation SOI
- SiGe/Strained Si On Insulator
- Ge On Insulator. This solution, a longer term solution, has also the potential to better match the introduction of a new class of gate insulators: the so-called high-k materials.

#### **Additional challenges related to strained Si and SiGe**

Epitaxy of appropriate donor substrates (quality, defectivity, throughput, ..)

SiGe and strained Si processing and relative immaturity compared to standard Si (cleaning, etching, thermal treatments, including oxidation, interface control, cross-diffusion, ..)

Wafer bonding schemes adapted to SiGe / Strained Si

#### **Additional challenges related to Ge**

While early demonstrations concerning the realization of GeOI substrates have been done, it still happen that Ge is definitely another material than silicon and that it will require in that respect several profound process module developments (Ge cleaning, passivation, annealing, etching). In that respect, any experience and background activity related to Ge processing is an added value.

Wafer bonding schemes adapted to Ge.

#### **Strong Points**

##### Crystalline orientation

Wafer bonding + layer transfer (European strength) have a strategic advantage to allow for mixed orientations;

Smart Cut preliminary demo already done (100, 110, 111, ..)

##### Strained Si On Insulator

Leadership for strained Si On Insulator wafers developments by layer transfer techniques (SOITEC on the industrial side, partnership with Siltronic, CEA-LETI, MPIHalle, QUB for institutes) : sSOI and SGOI manufacturing process by the Smart Cut technology;

sSOI unique solution for Ge-Free strained Si on insulator substrates

For layer transfer techniques, the donor substrates (epitaxial layers) are also of prime importance. There is a large number of leading actors in Europe involved in Relaxed SiGe/strained Si epitaxy

##### GeOI

Several teams have some experience of Ge epi and Ge processing in Europe (CEA-LETI, ST, IEF). Leadership for bulk Ge (UMICORE). For Ge On Insulator wafers developments by layer transfer techniques (SOITEC, CEA-LETI, UMICORE). On Ge processing (CEA-LETI, IMEC, UMICORE).



### Weak Points

Follower for other approaches to high mobility semiconductor on Insulator (condensation, SIMOX): No SIMOX actor. Japan and US leaders in condensation approach

Follower for other approaches for GeOI manufacturing (condensation).

Ge is a very specific material compared to Si, and will require specific process module developments which will mean an increasing cost.

### Conclusions and recommendations

- Improved mobility and SOI architecture is a strategic topic
- Three large potential solutions to develop for different and complementary terms (mid and long term): crystalline orientation, strained Si OI and GeOI
- This emerging European leadership in such a key and emerging area shall be maintained and reinforced.
- Wafer bonding + layer transfer techniques have as strategic advantage to be very flexible for Crystalline orientations control and mixing. Balancing the relatively low difficulty of implementation with the potential huge benefit, exploration and development of these solutions shall be a priority.
- Strained Si + SOI architectures is a strategic topic already on the ITRS roadmap.
- Good background and large number of leading actors in Europe involved in relaxed SiGe/strained Si epitaxy but also innovative relaxed SiGe formation techniques.
- Ge is a strategic topic for the long term part of the ITRS CMOS roadmap
- Thin films Ge on Insulator are needed if Ge wants to become mainstream technology.
- Leader technology and actors in Europe about Ge (bulk, epitaxy, layer transfer, smart Cut technology, Ge process module).

### 1.2.2.- New buried insulators

#### Comments

The formation of SOI materials with alternative buried insulators has been studied since at least 1990, having a profound increase in interest during the last years. The challenges are found in forming the advanced highly thermally conductive SOI materials without degrading electrical performance. Another problem is related to the stability of the buried oxide upon device processing in the SOI material. AlN and diamond may be oxidised during processing, causing minor problems with decreased thermal conductivity for AlN and catastrophic scenarios for diamond. Another "more mature" candidate to replace SiO<sub>2</sub> is Si<sub>3</sub>N<sub>4</sub>. Some early demos have already been reported (CEA-LETI), showing that beyond a single replacement the move to multilayered composite insulating stacks (SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>) can be realised. Thermal conductivity again can be improved but other device parameters optimization may also be concerned : breakdown voltage, global wafer bow and warp, buried insulator charge trapping properties, specific etch stop layer.

#### Strong Points

Leadership in Si<sub>3</sub>N<sub>4</sub> and Al<sub>2</sub>O<sub>3</sub> based buried insulators for SOI materials. Follower in other buried insulator.

Strong advantage of layer transfer techniques. Combinations with Smart Cut and or BSOI/BESOI for high quality SOI materials.



### Weak Points

Small activity on AlN

### European Groups

IMEP, Grenoble; France.

Soitec, Bernin, France.

### Conclusions and recommendations

- European groups have already a good position in the field and should be able to strengthen it.
- This type of SOI materials may be a potentially important product in the future, for different reasons: thermal management, bow/warp, buried insulator charge trapping properties.

### 1.2.3.- Complex SOI structures

#### Comments

The SOI material evolutions considered so far have been quite conservative as they stick to a simple stacking of an unique layer of semiconductor (mostly Si) on a buried insulator.

The potential is much larger. The spectra of possible more complex starting substrates contains a lot more enabling solution families that may address perfectly a large number of specific device architectures and applications. Among them can be found :

- Local and mixed SOI substrates. Such combinations on the same substrates open the doors to the use and combination of different technologies and functions on the same substrate : towards System On chip solutions. For instance, the combination of bulk and SOI transistors and devices can address smart power applications or even smart MEMS where MEMS and their electrical command can be closely packed.
- Buried structures: the substrates considered so far were blanket wafers. But techniques like layer transfer are also compatible with patterned structures: within the active layer that is transferred or contained within the new handle substrate. According to the latter scenario, it is possible to make buried patterned structure in a very flexible way. Examples of buried structures are capacitors (embedded memories), interconnects (early step towards 3D stacking), transistor gates (planar double gate transistors), ...
- Multiple SOI: the substrates considered so far were "single SOI" substrates in the sense that only one active semiconductor layer and one buried insulator were considered. But it is possible to realize double SOI substrates or to stack an even larger number of layers. This, combined with the possibility to incorporate patterned structures, opens a large door towards 3D stacking. It also opens the doors to specific applications such as optoelectronic for instance where multiple layers enables to realize Bragg reflectors and other mirrors, wave guides .
- Specific SOI for specific applications : The list of specific SOI substrates could be as long as the number of applications. Among them we can give an illustration through the following example: RF applications where CMOS would gain to enter more massively. In this kind of applications, one of the III-V big applications, the use of insulating substrates enables to lower high frequency substrate losses, cross talk , RF noise etc .. For Si, and especially SOI, at least two really different strategies have already been identified: the use of high



resistivity substrates or the introduction of ground planes (buried silicide for instance), both of them leading to specific developments at substrate level.

In all these cases, preliminary generic developments should be led at the substrate level in order to define the different technical opportunities to make the SOI substrate more complex. But in all these cases, the final specific substrate developments shall be driven by the applications, in close collaboration with the final end-users.

#### **Strong Points**

High flexibility of wafer bonding / layer transfer techniques to incorporate complex structures. Such techniques are the strong point of Europe

#### **Weak Points**

Many applications, many specific developments

High added value and innovative solutions but risky solutions

Lack of efficient collaborations with end-users, probably due to risks associated to technological breakthroughs.

#### **Conclusions and recommendations:**

- European groups have already a good exploratory position in the field and should be able to strengthen it.
- Unique, complex and high added value possible with layer transfer techniques
- Those developments, often related to specific device problems or specific applications shall be developed in close collaboration with end-users
- Funding Support should help minimizing the risks involved in these High added value / innovative solutions but risky solutions, as well as catalyzing substrate developers and final end-users collaborations.



### **1.3.- Material Characterizations**

#### **1.3.1 Electrical characterization**

##### **Comments**

The electrical properties of the starting SOI wafer determine the performance of the integrated circuits. The optimization of the wafer fabrication requires rapid feedback from characterization, which implies on-wafer measurements rather than time-consuming device-based information. However, the electrical characterization of SOI wafers is a difficult task due to the thinness of the film and complexity of the stacked structure. The pseudo-MOS transistor ( $\Psi$ -MOSFET) is a unique SOI device which does not need any technology at all. It is based on the upside-down MOS structure that is inherent in all SOI materials.

##### **Strong Points**

The expertise and leadership of European labs is recognized.

Development of new techniques SOI wafers. Many samples are available.

Support is needed to solve urgent issues related to the characterization of sub-10 nm thick film

##### **Weak Points**

Economic cost of the project

##### **European Groups**

SOITEC, France

CEA-LETI, France

IMEC, Belgium

UMICORE, Belgium

Chalmers, Göteborg, Sweden

##### **Conclusions and recommendations**

- Assessment of the economic viability of wafers with a diameter of 450mm. If this is positive then the development must begin immediately.
- Support is needed to solve urgent issues related to the characterization of sub-10 nm thick films. In particular, models are needed for parameter extraction with pseudo-MOSFET in ultra-thin films.
- Extend the principle of pseudo-MOSFET for other types of measurements: C-V and spreading resistance. Investigate the possibility of contactless measurements combining pseudo-MOS with optical methods (SHG or ellipsometry).



## **CHAPTER II. Devices. Characterization.**

### **2.1.- C-V measurements (including Zerst and DLTS)**

#### **Comments/Introduction**

C-V techniques can be used to characterise interface states and oxide charges both in the SOI material itself and using MOS capacitors fabricated in the SOI film. Capacitance measurements can be used to determine fixed oxide charge and interface states densities at both interfaces of the buried oxide. Generally interpretation of C-V data is fairly straight-forward using bulk theory in thick-fil partially depleted materials, while fully depleted material requires modifications in the theory. Using the Zerst technique (C-t), where capacitance transients are measured when the interface to be studied is pulsed from inversion to depletion, the average generation lifetime in the SOI material can be estimated. Deep Level Transient Spectroscopy can be applied to SOI materials, although the straight-forward conventional capacitance DLTS technique does not give reliable results on SOI materials, due to the high series resistance. Approaches to overcome this to give more accurate estimates of traps and states include conductance or current DLTS methods. Energy-resolved DLTS techniques may be necessary to use due to the continuous energy spectrum of the interface states and high levels of generation-recombination centres.

#### **European groups**

Many groups in Europe involved. IMEP has leadership in application to SOI structures.

#### **Strong points**

Considerable strength in model, adaptation and application to SOI devices.

#### **Weak points**

The European activities are fairly non-coordinated. Projects focused at characterisation lacking.

#### **Conclusions and recommendations**

The uses of C-V and C-t techniques are widely spread in Europe. Refinements may be needed for ultra-thin SOI films and non-standard SOI.

### **2.2.- Diodes : lifetime characterization**

#### **Comments**

The gated-diode technique, traditionally used for lifetime extraction in bulk Si devices, became more and more applicable for SOI devices. This technique is the only one, which allows extracting lifetime parameters directly from measurements on thin-film FD devices, which is of great interest for low-voltage, low-power applications. The great advantage of this method is also the possibility to separate the impact from volume and interfaces, and so to extract both volume generation (recombination) lifetime and surface velocities for top and bottom Si film interfaces.

#### **Strong Points**

Applicable to thin film FD SOI devices.

Allows to separate contributions from volume and from interfaces.

Applicable at high temperatures.

Very simple experimental setup.

Simplicity of the parameter extraction procedure.



The ability of characterizing front and back Si film interfaces and the film volume. very accurately and independently from each other.

**Weak Points**

Geometric limitation for gate-diode devices  
Needs for specific structures (i.e. gated diodes, or MOSFETs with body contact);  
Non-trivial interpretation in the case of SOI

**European Groups**

Sorin Cristoloveanu, ENSERG, Grenoble (France);  
A.Ionescu, EPFL, Lausanne (Switzerland)  
UCL (Louvain-la-Neuve, Belgium)  
ISP (Kyiv, Ukraine)

The scientific know-how and research groups possessing large expertise in this field exist in Europe.

**Conclusions and recommendations**

Gated-diode technique for extraction of carrier lifetime opens many perspectives, as it is applicable to thin-film FD devices, can be used at high temperature and allows to separate contribution from volume and surfaces generation (recombination). While the method appears rather simple for realization, the interpretation of results is not so simple in the case of SOI devices and demands a good background in this field. The gated-diode technique is used to determine GR parameters in thin-film-SOI MOS devices. A detailed analysis of the GR current behavior in thin-film SOI MOS devices can be performed using simulations of gate-controlled volume and surface GR components.

**2.3.- MOSFET characteristics and parameter extraction techniques**

**Comments**

The typical configuration of SOI transistors requires an adaptation of the conventional techniques used in bulk silicon MOSFETs and, in some cases, the development of new methods:

- Drain current vs. gate voltage curves.
- Saturation characteristics.
- Floating body effects.
- Coupling effects.
- Edge effects.
- Short-channel effects.
- Ultra thin gate oxide effects.
- Reliability aspects.

**Strong Points**

Adequate techniques and models, new mechanisms, reliability studies. Some advanced test devices are being fabricated.

**Weak Points**

Lack of software tools to extract parameters for the most advanced models.

**European Groups**

IMEP – Leadership  
LETI – Leadership  
IMEC – Significant contributor  
UCL – Significant contributor  
STMicro – Significant contributor



### **Conclusions and recommendations**

The European groups are very present in the international arena, where the competition is active. More focus is needed on extremely thin and short devices. New mechanisms emerge continuously and require revisited techniques. A European SOI characterization network, sharing state-of-the-art devices and appropriate techniques, is recommended.

### **2.4.- Transport measurements in MOS-like devices (including high/low temperature, magnetic field and stress)**

#### **Comments**

Transport measurements are essential for the analysis of the carrier mobility, doping behavior, band structure, quantum effects, etc. These measurements are difficult in thin SOI films (even impossible in fully-depleted films), without the use of a MOS structure which enables the modulation of the carrier concentration. In general, long-channel MOSFETs are inspected. A more sophisticated device is the MOS-Hall transistor, where additional lateral contacts allow performing Hall effect measurements. The advantage is that the carrier density and mobility are extracted independently and accurately.

#### **Strong Points**

Development of new techniques adapted to SOI devices. Good experimental facilities.

#### **Weak Points**

Limited sample availability and circulation between laboratories.

#### **European Groups**

IMEP – Leadership

LETI – Leadership

IMEC – Leadership

UCL – Key contributor

Univ. of Udine – Key contributor

### **Conclusions and recommendations**

The expertise of European labs is well known. Support is needed to solve urgent issues before the competitors (very active) succeed: accurate mobility characterization in sub-10 nm films, impact of quantum confinement and strain effects, optimization of thinning techniques, strain transfer methods, etc.

### **2.5.- Phonons in SOI**

#### **Comments**

Phonons in SOI are known to (i) determine the mobility limits at low temperature (acoustic phonons) and at room temperature (optical phonons) via electron-phonon scattering, (ii) act as probes for built-in strain due to lattice mismatch at the various interfaces: planar and around clusters and or grains, and (iii) to play a key role in thermal conduction.

There are very few laboratories working in this field. Critical mass has not been reached. Thermal conductivity in nanostructures is an emerging field in nanotechnology with potentially huge impact in simulations of devices and circuits.

#### **Strong Points**

Probably world-level leadership but effort too small to retain it.



### **Weaknesses**

Insufficient comparison of theory and experiment in device-like structures to extrapolate into device simulation. No experimental work in actual devices to determine thermal conductivity directly.

### **European Groups**

Leader: Univ. Montpellier II on strain in SOI assessment.

Leaders: Univ. College Cork (NMRC) and VTT on acoustic phonons in device-like SOI structures.

Contributors: Politecnico di Milano, Univ. Paul Sabatier, Univ. Granada

### **Conclusions and recommendations**

Acoustic phonon studies of SOI structures is an emerging field needing strong support to harvest the benefits to improved SOI device performance based on phonon engineering.

## **2.6.- Charge pumping**

### **Comments**

The Charge Pumping (CP) method is very efficient for the evaluation of interface traps that govern the quality of MOS circuits. The adaptation of CP to SOI transistors requires a contact to the Si film: either 5-terminal MOSFETs or gate-controlled p-i-n diodes may be used. In fully depleted devices, special SOI coupling effects occur: the pulsing of the front gate results in a scanning of the back surface potential which enables the pumping of some of the back interface traps. Another parasitic CP current is due to "dimensional effects", which happen in long devices or if the rise/fall times of the pulse are too short.

### **Strong Points**

Model, adaptation and application to SOI devices

### **Weaknesses**

### **European Groups**

IMEP – Leadership

IMEC – Leadership

### **Conclusions and recommendations**

The Charge Pumping technique is available in Europe. Developments are needed for extra thin SOI films and gate oxides, and for measuring the buried interface properties from front-gate CP experiments.

## **2.7.- Electro-luminescence techniques.**

### **Comments**

Electron-luminescence techniques have been used to analyse in detail hot carrier effects in SOI technologies and to compare hot carrier effects in bulk and SOI technologies. The relationship with hot-carrier degradation has also been studied. Self heating in SOI has also been analyzed with EL.

### **Strong Points**

Spectrally resolved characterization and physically based photon emission simulation capabilities at the device level.

Spatially resolved ultra-fast circuit imaging. Circuit design testing and failure analysis.

Integral light intensity characterization at the device level



## Weaknesses

### European Groups

DIEGM, Univ. of Udine, Italy  
Dept. of Physics, Univ. of Parma, Italy  
IMEP, Grenoble, France

### Conclusions and recommendations

In recent years, voltage scaling has reduced the emphasis on hot carrier effects as the source of the dominant MOSFET (including SOI) reliability concerns. However, hot carriers are still present in modern technologies and they are relevant for PD and FD SOI's also as the source of substrate holes. EL measurements have been historically exploited mostly in relation to hot carrier and degradation analysis. However, the technique is much more general and represents a valuable source of data to verify and calibrate carrier transport models in semiconductor devices. EL studies can help device analysis as a mean to characterize carrier distribution functions, in particular in the low voltage, presumably quasi-ballistic regime. The relative importance of different emission mechanisms at low voltage and in particular in SOI devices is not yet fully assessed. From the experimental point of view, sensitive detectors for the energy range below 1eV would be desirable in view of the reduced supply voltages of present and future devices.

## 2.8.- Noise and fluctuations.

### Comments

The noise reflects the current fluctuations brought about by random variations in carrier number and/or mobility. Excess noise in SOI transistors is generated by the floating body effects, induced by either impact ionization or gate tunnelling current (GIFBE). Another special feature in SOI is the interface coupling which may result in a superposition of noise generated at both interfaces. The appropriate biasing of the front and back gates enables to isolate a particular mechanism or a region from the surroundings, in order to measure the noise generated solely by that source.

### Strong Points

Models, adaptation and applications to SOI devices. Recent developments.

### European Groups

IMEP – Leadership  
IMEC – Leadership  
Inst. Semiconductors, Kiev - Contributor

### Conclusions and recommendations

The noise spectroscopy is an elegant method to discriminate various defects and mechanisms. This technique is available in several European labs which maintain an active leadership. New developments (extra thin SOI films, tunneling gate oxides, quantum related transport, etc) deserve being supported.



## 2.9.- Transient and history effects

### Comments

In case of Partially depleted transistors, the internal floating body potential can not be externally fixed, as for Bulk or Body-contacted SOI transistors. This means that the body charge (and hence its potential) is fixed by the voltages applied on the external nodes, and by considering the Kirschoff law at the internal floating body node. This body potential is thus dependent on the external biases applied and is also time related. This leads to the well known 'transient and history effects'. The threshold voltage of the SOI MOSFET (and hence the performance) being modified by the body voltage, it becomes obvious that an accurate modelling of this internal body potential is essential for the correct modelling and design of SOI transistors and circuits. This floating body potential is fixed by a balance between generation and recombination mechanisms.

### Strong Points

History effects on Partially depleted technology well developed.

### Weak Points

History effects on advanced single and Multiple-gate Fully depleted technologies.

### European Groups

IMEP: Significant Contributor

LETI: Significant Contributor

ST: Significant Contributor

### Conclusions and recommendations

European groups contribute significantly on the field of transient effects and history effects characterization for Partially Depleted technology. Only few analysis are performed on single-gate and multiple-gates Fully Depleted technologies. This last point should be developed significantly.

## 2.10.- Floating-body effects (including gate-induced FBE and Meta-Stable Dip)

### Comments

Due to the fact that the internal floating body potential can not be externally biased in SOI transistors, its value is fixed by all the carriers injected in the body region. Balance between impact ionization current, Gate Induced Drain Leakage current, junction currents determines the value of this body potential by applying the Kirschoff law in DC mode. In transient mode, dynamic currents contribute to the injection of charges in the body, modifying the body potential value. All the previous mentioned currents must be accurately characterized and modelled, in order to correctly simulate the floating body voltage that reflects the performance of SOI transistors.

### Strong Points

There exist characterization methods for bipolar transistors

### Weak Points

Mostly only quasi-static characterization of floating body effects: not enough dynamic characterization

### European Groups

IMEP: Significant Contributor

IMEC: Significant Contributor

LETI: Significant Contributor



### **Conclusions and recommendations**

European groups contribute significantly on the field of floating body effects characterization for partially depleted and fully depleted SOI technologies. Most of the characterizations are quasi-static methods, where the time constants are quite long. University of Southampton is the only one to publish on dynamic characterization of floating body effects. That kind of methods must be developed in Europe. The MSD effect has potential for developing capacitor-less DRAMs. This action should be encouraged as being industrially viable.

### **2.11.- Ultra thin film effects in MOSFETs**

#### **Comments**

The scaling of Fully Depleted SOI transistors induces a thinning of the SOI layer. A ratio of 3 to 5 is commonly adopted to ensure good performance for the transistors. This means that SOI films as thin as 5nm must be used for gate length as short as 30nm. Such thin layer modifies significantly the electrical properties of the SOI transistors. Firstly, a mobility reduction has been observed when we reduce the SOI thickness below 10nm. Secondly, quantum effects occur in thin SOI film.

#### **Strong Points**

Coupling effects in thin SOI layers are well characterized.

#### **Weak Points**

Not enough activity on quantum related effects.

#### **European Groups**

IMEP – Leadership

LETI – Leadership

UGR – Important contributor.

### **Conclusions and recommendations**

The contribution of European groups is not a leadership activity. Main contribution is still coming from Japan, where ultra-thin transistors are available since many years. Experimental characterization of quantum related effects must be increased in Europe, as experimental transistors are now available in Europe with SOI layer thinner than 10nm.

### **2.12.- Self-heating (+ High T<sup>a</sup>)**

#### **Comments**

The dielectric isolation (when SiO<sub>2</sub> is used as buried insulator) give rise to a drawback due to the low thermal conductivity of the buried insulator. As a consequence the temperature in SOI devices may rise to values higher than in bulk devices due to self-heating effects. Both the limited thermal conduction from the SOI film to the substrate heat sink and the reduced capacity for lateral heat spreading may affect the device performance due to reduced mobility.

#### **Strong Points**

Extraction of thermal parameters. Self-heating in power devices. Novel SOI materials.

#### **Weaknesses**



### **European Groups**

Philips Research Leuven – Strong contribution/leadership  
Uppsala University and Chalmers University - contributors  
IMEP/LETI  
Queen's University

### **Conclusions and recommendations**

There are fairly good European activities both on materials manufacturing and characterisation and on device characterisation. Techniques for measuring the thermal conductivity of various buried insulators should be developed. An increased collaboration between the groups would probably considerably strengthen the European activity.

## **2.13.- Special device characterization (multiple gates, high voltage FETs, etc)**

### **Comments**

Non planar multiple gate SOI transistors appear to be one of the most interesting device for the future. Such kind of transistor will only replace the standard planar transistors, if the quality of the vertical channels is as good as the one of the planar transistors. So the vertical edges of the Fin must be carefully characterized in term of mobility and interface quality.

### **Strong Points**

Coupling effects in FinFET are well known as well as 4-gate transistors.

### **Weaknesses**

Not enough transistors available for electrical characterization.

### **European Groups**

IMEP – Leadership  
UGR – Significant contributor

### **Conclusions and recommendations**

The contribution of European groups is not a leadership activity. The process of FinFET transistors in Europe should help significantly the development of characterization methods. The coupling effects in multiple-gate transistors should be investigated for devising conceptually new digital and analog circuits.

## **2.14.- SOI High Voltage Transistor Characterization.**

### **Comments**

High voltage MOS transistors formed by a gate and a drain drift region. Due to the electrical properties of the drift region modeling of the characteristics is not trivial. We use a BSIM-MOS model with a drain resistance subcircuit for modeling the drift region effects.

### **Strong Points**

Accurate models. Models and extraction strategies available for several technologies.

### **Weaknesses**

Simulation time.  
Complexity



### **European groups**

Automacs IST-project: Advanced Unified Lateral DMOS Transistor Model for Automotive Circuit Simulation (partners: AMI Microsystems, Belgium; Bosch GmbH, Germany; IMEC, Belgium; SILVACO, France).

Many companies offering high-voltage/ high-power MOS devices

### **Conclusions and recommendations**

High voltage modeling is well understood. Support is needed for a more compact formulation of the models and further development for advanced simulation techniques.

## **2.15.- . High Voltage Characterization During Production**

### **Comments**

The requirement to measure high voltage comes from SOI high voltage technology providing drain to source breakdown voltages of more than 700V. To secure the quality of each wafer and to monitor the technological process a enhanced high voltage monitoring test systems is available within standard production environment.

### **Strong Points**

Development of new techniques for SOI wafer production measurements.

### **Weaknesses**

Add more characterization parameters to automated test. Be sure, that the required measurement time is optimized.

### **European groups**

### **Conclusions and recommendations**

The installation of novel characterization methods within standard production environment is used for characterization work of high voltage devices and can replace time expensive manual characterization. Time optimized routines are required.



### **CHAPTER III. Devices. Fabrication Technology**

#### **3.1.-SOI CMOS TECHNOLOGY**

##### **3.1.1.- Field isolation: LOCOS, mesa, trench isolation**

###### **Comments**

Vertical device isolation is intrinsic to SOI technology; this is one of the main reasons why SOI technology is gaining momentum with respect to the conventional bulk silicon technology. Therefore, the techniques generally used are the lateral device isolation solutions that are necessary to fulfil the complete isolation of devices needed in IC (LOCOS (Localized oxidation of silicon), MESA, Trench Isolation (TI))

###### **Strong Points**

LOCOS

Smooth surface topology. Easy to implement and its cost is low.

MESA ISOLATION

No width loss. This technique allows high integration density.

TRENCH ISOLATION

Sidewall liner oxidation can be performed. It allows tighter active area pitch. Creates more planar front-end.

###### **Weak Points**

LOCOS

Bird's beak. High tensile nitride stress can generate dislocations in the silicon.

MESA ISOLATION

Gate over-etching gate dielectric integrity at mesa sharp corners sidewall parasitics

TRENCH ISOLATION

TI strain-induced device degradation micro-scratches and gouges. Control of over and under polish.

###### **European Groups**

CEA-LETI (France), IMEC (Belgium) , VTT (Finland), STMicroelectronics, Infineon

###### **Conclusions and recommendations**

The techniques presented here are the lateral device isolation solutions that are necessary to fulfil the complete isolation of devices needed in SOI IC (LOCOS (Localized oxidation of silicon), MESA, Trench Isolation (TI)). The vertical device isolation is intrinsic to SOI technology. The main difficulties found in relation to these techniques are: LOCOS (bird's beak, high tensile nitride stress can generate dislocations in the silicon). MESA ISOLATION (gate over-etching, gate dielectric integrity at mesa sharp corners, sidewall parasitics). TRENCH ISOLATION (TI strain-induced device degradation, micro-scratches and gouges, control of over and under polish).

##### **3.1.2.- Channel doping and mobility enhancement techniques**

###### **Comments**

Increased doping concentration in bulk or PDSOI devices to further scale down the gate length results in degradation of mobility. Reduction of the supply voltage to prevent increased field and non scalability of  $V_T$  and  $T_{ox}$  to maintain stand-by power requirements reduces the gate overdrive  $C_{ox}(V_{DD}-V_T)$ . High k dielectric will likely further degrade the transistors performance. Thin film devices such as FDSOI or DG SOI uses



very thin silicon film with reduced mobility due to increased surface roughness scattering. Undoped films make the transistors operate at lower electric field and somewhat compensate for the mobility loss. Few techniques used to increase the channel mobility are the following:

- Strain engineering: process- or substrate-induced strain
- Crystal orientation effects
- New channel materials such as Ge
- SiGe SD stressor

#### **Strong Points**

Techniques available to increase the channel mobility:

- Strain engineering: process- or substrate-induced strain
- Crystal orientation effects
- New channel materials such as Ge
- SiGe SD stressor

#### **Weak Points**

Compressive stress from STI results in nMOS performance degradation.

The quality of the strained-Si silicon layers, however, can be worse than the conventional ones.

##### **Crystal Orientation Effects**

Limited scalability of bulk devices and increased process complexity.

##### **Germanium On Insulator**

Compatibility with a stable gate dielectric

#### **European Groups**

CEA-LETI (France), IMEC (Belgium), VTT (Finland), STMicroelectronics, Infineon

#### **Conclusions and recommendations**

- Very high European Research Activity in high-mobility channels.
- Processing issues specific to the strained and Ge, or C, containing material, will need to be addressed:
  - ultra-thin (1 nm) gate oxides, effects of strain and Ge content on oxidation rate and reducing gate leakage
  - laser doping for ultra shallow junctions, lateral channel profiling
  - device isolation: STI, self aligned STI
  - smart-cut and wafer bonding processes for SSOI
- Hard work still necessary in the characterization and simulation of these devices.
  - Material and device characterisation are crucial to understanding, and vital for making progress.
  - New scattering models have to be developed.
- These devices must be incorporated into standard CMOS production. However, within Europe there is considerable experience of putting research material through standard process lines and developing new process modules.

#### **3.1.3.- Source and drain engineering: silicide source and drain, elevated source and drain**

##### **Comments**

The fabrication of source and drain structures in SOI devices is a very important issue. The fabrication in partially depleted devices implies the use of techniques different to the ones used in the case of fully depleted devices. Silicide and elevated source and



drain are the main proposals to deal with the difficulties found in the fabrication of SOI devices.

#### **Strong Points**

Elevated S/D, reduction of SD junction resistance and less voids formation.

#### **Weak Points**

Elevated S/D (silicon shrink, they agglomerate into silicon islands and their shape changes after thermal treatment)

#### **European Groups**

CEA-LETI (France), IMEC (Belgium), VTT (Finland), STMicroelectronics, Infineon

#### **Conclusions and recommendations**

There are open questions that have to be addressed such as: voids formation during silicidation, increased SD junction resistance when the silicide thickness reaches the silicon film thickness, very thin Si films are quasi-stable, agglomerate into silicon islands.

### **3.1.4.- Gate stack, gate electrode materials, gate dielectric**

#### **Comments**

Due to the aggressive scaling of the gate dielectric, the gate leakage is becoming unacceptably high ( $> I_{off}$ ), requiring the use of high k dielectrics. In this section, high k dielectrics are discussed and the main issues to be solved described: fringing field (FIBL) and loss of control of the channel by the gate, mobility degradation, VT instabilities and reliability issues. On the other hand, for the elimination of polydepletion and boron penetration, metal gate electrodes will likely be needed.

#### **Strong Points**

High k dielectric can reduce gate leakage current by 3-4 decades.

Metal gates eliminate boron penetration problem and can decrease gate resistance as gate height is scaled.

#### **Weaknesses**

High K dielectrics produces mobility degradation, VT instabilities and reliability issues.

Large k and large dielectric thickness result in fringing fields.

Totally silicided gates: Incomplete silicidation, local silicidation rate can vary highly depending on nucleation conditions and gate dielectric reliability

#### **European Groups**

CEA-LETI (France), IMEC (Belgium), VTT (Finland), STMicroelectronics, Infineon

#### **Conclusions and recommendations**

The main difficulties to be solved in this field are: gate dielectric reliability, phase uniformity of the NiSi throughout the structure, local silicidation rate that can vary highly depending on nucleation conditions, etc.



### **3.2.- High Voltage Devices**

#### **3.2.1.- LDMOS processes**

##### **Comments**

A strong driving force in the field of microelectronics is to increase the functionality of the chips by integration circuits and devices with different functions. SOI enables easier integration of high voltage devices and low voltage circuits on the same silicon chip. One field that can take advantage of this is the automotive electronics, where there is a strong trend to increase the level of integration.

##### **Strong Points**

Major European industrial player, with mature SOI-LDMOS processes. Market share in automotive electronics and audio amplifiers

##### **Weak Points**

Small academic activity, compared to USA and Korea

##### **European Groups**

Philips Semiconductor - leadership

##### **Conclusions and recommendations**

European academic research can be strengthened in this field. It may be worthwhile to exploit the RF-performance of SOI-LDMOS transistors. A complete integrated (CMOS/LDMOS) front-end power amplifier for wireless communication might be possible using SOI-technology.

#### **3.2.2.- Vertical SOI High Voltage Processes**

##### **Comments**

European groups and industries have demonstrated vertical high-voltage (>650 V) devices on thick SOI-layers. Increased level of integration is therefore possible.

##### **European Groups**

X-FAB - commercial high-voltage SOI processes (leader)

Uppsala University – process and device development (contributor)

##### **Strong Points**

European foundry exists.

Lot of academic knowledge has been built up.

##### **Weaknesses**

Limited commercial interest as of today.

##### **Conclusions and recommendations**

The field might be promising for further exploitation. In particular automotive electronics may be targeted, considering the several automotive industries in Europe.

#### **3.2.3.- Bipolar SOI processes**

##### **Comments**

The full electrical isolation of devices offers benefits such as reduced junction capacitance, improved on-current for given off-current, elimination of latch-up, higher temperature operation, and mixed analogue and digital circuits. For bipolar transistors on SOI, a significant reduction in the collector-substrate capacitance is achieved. When combined with trench isolation, a further reduction in capacitance and increased packing density is obtained. This results in higher frequency performance and/or lower



power dissipation. The overall performance of bipolar SOI technology continues to increase primarily due to the aggressive vertical and lateral scaling capability of silicon technology. State-of-the art results have been achieved using different concepts of bipolar vertical and lateral design. Special emphasis is on SiGe HBT device – a leading contender among the Si-based approaches for high frequency applications. From Europe, a UK consortium group (comprising the Universities of Liverpool, Queen's Belfast, Southampton, Surrey, and the Imperial College (with industrial partners)) has contributed to the development of the bonded SOI SiGe HBT platform, while STMicroelectronics and Bordeaux University was the first to fabricate SOI SiGeC HBTs. Significant results in the area of BiCMOS integration were achieved by IHP, Germany.

### **European Groups**

Significant Contributor: UK consortium – SiGe HBTs on wafer bonded substrates  
Leadership: Queen's University Belfast, UK – crosstalk suppression (GPSOI, silicide SOI etc.)  
Significant contributor: Southampton University – lateral SOI SiGe HBTs  
STMicroelectronics, France  
+ Bordeaux University – SiGeC HBTs and SiGe HBT on a thin film SOI  
Royal Institute of Technology, Kista, Sweden + Infineon Technologies, Sweden – work on different isolation schemes  
The University of Louvain, Belgium - work on passivating the substrate surface of HR Si wafers  
Uppsala University, Sweden – LR-SOI  
IHP, Germany – SOI BiCMOS  
Significant work on cross-talk suppression (GPSOI, HR-SOI, LR-SOI).

### **Technical challenges**

- Main disadvantages of standard SOI substrates are that (i) the buried oxide layer has poor thermal conductivity and so, self-heating can be a problem, and (ii) at high frequencies the buried oxide is electrically transferred resulting in signal transmission losses and crosstalk problems. A further disadvantage is large collector resistance.
- The major constraint for bipolar design on thin film SOI is the limited film thickness for the device to be integrated.
- The system-on-a-chip solutions necessitate efficient isolation of the different circuit blocks. To reduce the transmitted noise through the substrate (crosstalk) various methods have been developed: HR-SOI, GPSOI, LR-SOI.
- SOI BiCMOS integration is a major challenge.

### **Strong points**

- Europe shows excellent work on crosstalk suppression (UK, Sweden);
- First demonstration of SiGeC HBT on SOI and lateral SOI SiGe HBT in Europe (France and UK, respectively);
- Novel scheme for BiCMOS integration (Germany).

### **Weak points**

- Lack of continuity and funding
- Uncertainties around take-up from industry



### **Conclusions and recommendations**

Pockets of expertise on SOI-HBT and related technology exist in Europe but greater engagement with industry is required for any exploitation other than generic training.

### **3.3.- RF and Power Devices**

#### **3.3.1.- SOI LDMOS RF-Power Transistors**

##### **Comments**

LDMOS transistors on SOI-substrate, on the other hand, have the potential to offer both better RF-performance (especially in terms of power efficiency), but also a higher level of integration, thereby enabling one-chip radio power-modules. Direct comparison between bulk and SOI-LDMOS, show better efficiency for the SOI devices due to reduced parasitics.

##### **Strong Points**

Several European industrial players (Philips, Infineon, ST Microelectronics) have established RF-LDMOS on bulk, and have the competence to transfer to SOI-LDMOS.

##### **Weaknesses**

Small industrial and academic activity in Europe.

##### **European Groups**

No significant European contribution as of today

### **Conclusions and recommendations**

It will be difficult to compete with commercial bulk LDMOS with SOI-LDMOS, unless the performance of the SOI-LDMOS is very much improved. A more realistic opportunity for SOI is to demonstrate RF-power LDMOS integrated with CMOS, which would enable smarter power amplifier modules, both for handset and base station applications.

### **3.4. Optical SOI technology**

#### **3.4.1. SOI waveguides**

##### **Comments**

SOI photonic crystals slabs have been fabricated by soft UV-nanoimprint lithography over large areas with sub 100 nm feature sizes down to a depth between 100 and 200 nm. The nanoimprinting step needed a tri-layer stamp. The results were successfully simulated

##### **Strong Points**

Compatibility with the CMOS fabrication process. Possibility of using low cost non-traditional lithography is increasing.

##### **Weaknesses**

Strong demands on fabrication accuracy.

Cost.

##### **European Groups**

Leadership: IMEC

Contributors: CEA, VTT, Technical University of Denmark COM, CNRS-LPN



### **Conclusions and recommendations**

In a couple of years, Silicon-on-Insulator has become a major platform for photonic integrated circuits. Three European projects has a particularly interest in waveguide devices: European Network of Excellence FP6-ePIXnet, the European research project on on-chip optical interconnect FP6-PICMOS and the European Space Agency project on Multi Gigabit Optical Backplane Interconnections. The field is characterized by a strong competition around the world. Cost-reduction strategies are in progress to make this concept development viable. Developments are needed for the optimization of single UV-lithographic step. The EU-Integrated Project “Emerging Nanopatterning methods (NaPa)” is developing alternative nanofabrication methods at wafer scale suitable for photonic crystal components.



## **CHAPTER IV. Devices. Physics.**

### **4.1 Classical SOI MOSFETs.**

#### **Comments**

SOI integrated circuits consist of many (millions) of SOI devices formed in a thin Si layer. Each transistor is dielectrically isolated from the underlying Si substrate by the buried oxide layer and from other transistors by shallow trench insulation. There are several peculiarities common to all types of SOI, which makes this technology competitive and puts it into the mainstream of commercial development and applications:

- The vertical isolation of the active Si film from the Si substrate by means of a buried oxide layer removes the well known parasitic effects common to bulk devices such as leakage currents, radiation-induced photocurrents, latch-up effects.
- The source and drain contacts are extended down to the buried oxide, lowers the leakage current and reduces the junction capacitance. This offers the opportunity to fabricate CMOS circuits with lower power consumption both in standby and operation mode, improved speed and for a wider temperature range.
- SOI transistors are better suited to overcome the scaling challenges. Contrary to the bulk-Si case, the SOI Si film thickness can be reduced together with the device shrinking. It reduces the drain-to-body field penetration and improves the control of the potential and the charge in active Si layer and reduces short-channel effects.

Repeated comparisons demonstrate that the operation at similar voltage provides a gain in performance of about 30%, as compared to bulk-Si. On the other hand, operation at similar low-power dissipation roughly doubles the gain. In general, SOI circuits of a certain generation have a performance similar to that of the next generation of bulk-Si. Combining strained Si with SOI technology opens new opportunities to address the 65 nm and beyond technology nodes.

Different criteria may be chosen for SOI type classification. From the physics point of view, it is convenient to divide SOI devices according to the regime for the Si body: partially depleted (PD), fully depleted (FD), ultra-thin body (volume inversion), and accumulation mode SOI.

#### **4.1.1 Partially depleted SOI.**

##### **Comments**

In partially depleted SOI devices the depletion region does not extend through the whole Si film. A neutral, not-depleted part of Si film is not connected and called floating body. Floating body effects are intrinsic to PD SOI transistors. They are determined by the floating body potential, which can be changed by impact ionization or gate-to-body tunneling. Floating-body effects may be beneficial or problematic, depending on particular applications.

##### **Strong points**

- Current increase at saturation is known as the kink effect. The kink effect is triggered by impact ionization. The generated majority carriers are accumulated in the floating body region. The body potential raises leading to threshold voltage lowering and higher saturation current.

- Ability of the floating body to store the charge is exploited in exploratory 1T-DRAM architectures without a storage capacitance.
- When a contact between the body and the gate is introduced, a dynamic threshold (DT) MOS is created. DTMOS possesses nearly ideal subthreshold characteristics, a reduced body effect and improved current drive.

#### **Weak points**

- Transient variations of body potential, threshold voltage and current can occur. It causes history and memory effects and may also lead to dynamic instabilities.
- A parasitic bipolar transistor consisting of source, floating body, and drain can be formed and has to be taken into account for circuit design.
- Self-heating effects are more pronounced due to the low thermal conductivity of the buried oxide.
- Special adjustments must be made in order to simulate PD SOI MOSFETs with standard transport models.
- Due to lateral depletion, short-channel PD FETs may turn into the full depletion.

#### **Conclusions and recommendation**

- PD FETs exhibit superior performance as compared to their bulk counterparts.
- Additional advantages arise from using the floating body node. The dynamic threshold MOSFET with improved subthreshold and current characteristics is an example.
- Special adjustments to standard transport models, like hydrodynamic or six-moments models, used in numerical device simulators, are required in order to address correctly the floating body effect.

### **4.1.2. Fully Depleted SOI**

#### **Comments**

Full depletion occurs when the depletion region extends over the whole Si film. The floating body effect disappears. Due to the full depletion the front and back interface potential become inter-related. The second surface layer at the buried oxide interface can be activated. Coupling between the front and the back channels develops. The FD SOI MOSFETs characteristics start to depend on the substrate bias adjusted with the voltage applied to the back gate. It increases the variety of options for device design and opens new directions for performance optimization.

#### **Strong points**

- Small leakage current, weak temperature sensitivity of the threshold voltage and an ability to sustain soft errors due to radiation prompts for the usage of FD SOI circuits at temperatures beyond the room temperature as well as in extreme environments.
- Excellent coupling between the gate voltage and the inversion charge results in improved current characteristics and subthreshold slope.
- Possibility to generate new memory effects such as meta-stable dip due to induced floating body effects.
- Use of low-permittivity buried oxides or silicon-on-nothing technology allows reducing greatly the fringing field penetration into the buried oxide and related short-channel effects.

#### **Weak points**

- Reliability of short-channel MOSFETs via induced degradation of the front channel properties due to degradation of the back interface or the buried oxide, induced by hot carrier injection into the oxide.



- Self-heating leads to on-current lowering.
- Potential of the back interface may be inhomogeneous, from the depletion in the middle to a weak inversion near channel ends. This effect may degrade the swing.
- Short-channel effects resulting in threshold voltage roll-off, such as drain-induced barrier lowering effect (DIBL) and drain-induced virtual substrate biasing (DIVSB) due to an increase of the potential at the back interface caused by the fringing field in the buried oxide.

#### **Conclusions and recommendations**

- Superior channel control as compared to PD SOI FETs makes a FD SOI FET a good candidate for high-performance, low-power dissipation devices beyond the 65 nm technology node.
- More parameters, like the Si film and buried oxide thicknesses, substrate doping and independent ground plane biasing are available for performance optimization of FD SOI FETs.

#### **4.1.3. Ultra-thin-body SOI**

##### **Comments**

When the Si thickness of FD MOS is further decreased, the front and back inversion channels are approaching each other, bringing the whole Si film into inversion. The volume inversion is responsible for superior characteristics of thin-body SOI MOSFETs. Due to the volume inversion, the minority carriers are flowing in the middle of Si film, experiencing less scattering with rough interfaces. The volume inversion improves the mobility and transconductance and decreases low-frequency noise. Double-gate or gate-all-around architectures exert an excellent channel control. In overall, double-gate thin-body SOI FETs are considered as an efficient solution for MOSFETs below 10 nm, which allows to gain speed and to save energy.

##### **Strong points**

- Improved performance due to volume inversion.
- Possibility to use undoped Si body reduces the impurity scattering and enhances the mobility.
- Excellent channel control by the gates.
- Double gate or gate-all-around solutions reduce short channel effects dramatically due to ideal electrostatic channel control.

##### **Weak points**

- Threshold voltage is not controlled by the Si doping. Using metal gates is mandatory to control the threshold voltage.
- Rapid mobility degradation if the Si film thickness is decreased below 3.5 nm.
- Atomic-level Si thickness control is required in order to avoid surface roughness mobility degradation.
- Rapidly increasing sensitivity of transistor characteristics to unavoidable random spreads of their geometrical parameters (Si film and oxide thicknesses, gates length and alignment) due to fabrication uncertainties with scaling FETs down.
- Potentially strong sensitivity of FET characteristics with respect to few dopant or interface trap random distribution in ultra-scaled devices.

### Conclusions and recommendations

- Double-gate, triple-gate, or gate-all-around ultra-thin body SOI MOSFETs show nearly an ideal channel control and reduced short-channel effects and are considered as perfect candidates for breaking the 10 nm FET scaling limit.
- Recently shown mobility enhancement in 2.5 nm thick Si films due to stress, which was comparable to the enhancement in bulk Si, demonstrates the advantage combining ultra-thin body SOI with stress technology.
- Extremely tight tolerance with respect to parameter variations, like Si and oxide thickness fluctuations, gate length, gates alignment, etc. are the most serious technological problems, which has to be solved to prop the ultimate success of ultra-thin body SOI MOSFETs.

#### 4.1.4. Accumulation-mode MOSFETs

##### Comments

Thin-body SOI is operated in accumulation mode. Similar to thin-body SOI FETs in volume inversion mode, in accumulation the current is flowing across in the whole Si body, which is beneficial to increase the mobility by moving the current carrying channels away from rough surfaces.

SOI biased into accumulation opens unique opportunities for new device structures. A complimentary room temperature single-electron/hole action was recently demonstrated in nanosize narrow-width FD SOI MOSFETs. A single-electron island was formed in the floating body by biasing SOI to accumulation. The island was weakly coupled to the source and the drain via the Zenner tunneling process providing single electron operation regime.

Another interesting idea is the 4-gate transistor, which uses all the contacts available as the gates to modulate the conduction path by MOS junction FET effect. The independent action of all the four gates opens new perspective for conceptually new quaternary logics.

##### Strong points

- Better short-channel effects than in FDSOI is predicted
- Higher threshold voltage than in FDSOI.
- No effects caused by the depletion of poly-Si gate.
- Because of the body current conditions the low-frequency noise level is lower.

##### Weak points

- Slightly worse subthreshold characteristics compared to FDSOI
- More difficult process of growth of gates N or P polygates for p or n channels.

##### Conclusions and recommendations

- Vast potential of SOI MOSFETs in accumulation mode for conventional and advanced applications, like single-electron room temperature operation or quaternary logics, is yet to be revealed.



## 4.2.- HIGH VOLTAGE AND POWER DEVICES

### Comments

Power devices are crucial for the commercial success of SOI technology in the fields of automotive and telecommunications (RF). LDMOS transistors up to 1200 V compatible with all the existing SOI substrates have to be developed since LDMOS is the unique power structure with optimal electrical performances in SOI substrates. System-on-Chip and Smart-Power applications on Thick, Thin and Ultra-Thin SOI substrates for transportation and mains operated circuits require power switches with maximum current capability and the subsequent protection power devices with lateral architecture (LTVS, LZener) The feasibility of Ambient Intelligence technologies is attached with the availability of reliable power devices suitable for extreme conditions operation. The know-how in multi-gate MOSFET structures will have to be transferred to power devices for their compatibility with advanced CMOS technologies.

### Strong points

Mature Bulk power LDMOS technology and good know-how on SOI power LDMOS device architecture and SOI process technology for feasible future integration in all the available SOI substrates.

### Weak points

Very few research groups in Europe dedicated to power SOI.  
Current capability limitation and excessive temperature increase.

### European Groups

Philips SC, The Netherlands.  
CNM-CSIC, Barcelona, Spain.  
Uppsala University, Sweden.

### Conclusions and recommendations

- Renewed European research effort dedicated to power devices for new SOI substrates has to be done.
- The success of future Ambient Intelligence technologies is directly attached to the improvement of power switches on SOI

## 4.3.- RF DEVICES

### 4.3.1. SOI bipolar transistors

#### Comments

SOI bipolar technology allows the complete dielectric isolation of the device. This approach reduces parasitic capacitance to substrate, leakage currents, and device size. The SOI substrate eliminates parasitic substrate transistors and latch-up and has the ability to reduce crosstalk, particularly when combined with buried groundplanes. Regarding vertical SOI SiGe HBT technology contribution has been given from a UK consortium group – the bonded wafer technology resulted in 20 dB reduction in crosstalk. A major challenge for fabricating ultra-thin base layers is the control of transient enhanced diffusion (TED) of dopants, which occurs during annealing of implantation damage. To maintain the ultra-fast transit time across the base, carbon can be introduced to reduce boron TED leading to SiGeC HBT technology. The first high-speed SOI SiGeC HBT has been demonstrated recently by a European group (France). As for lateral bipolar transistors, SOI technology is readily adapted due to its capabilities to overcome the main difficulties namely, (i) definition of a lateral thin base,



(ii) definition of a fully aligned base contact, and (iii) device isolation. First lateral SOI SiGe HBTs have been reported by a European group too (UK).

**European position on the field**

Table 1 summarizes European research activity regarding bipolar SOI transistors. HBT technology is of primary importance. In particular, novel concepts have been introduced by UK groups, such as SSOI (tackling collector resistance as a key issue in SOI SiGe HBTs) and CLSEG (confined lateral selective epitaxial growth used for lateral SOI SiGe HBTs). STMicroelectronics and Bordeaux University, France, have demonstrated for the first time SOI SiGeC HBT structure – results have been published this year.

European group	SOI bipolar transistors platform & associated activities
UK consortium	Bonded SOI SiGe HBT
Queen’s University Belfast, UK	SSOI (silicide SOI) process for SOI SiGe HBT
STMicroelectronics and Bordeaux University, France	SOI SiGeC HBT
Southampton University	Lateral SOI SiGe HBT; processes for HBT growth: SEG, NSEG, CLSEG

Table 1: European research activity in the field of SOI bipolar transistors

**Technical challenges**

- Minimisation of collector resistance as a key issue in SiGe HBTs on SOI.
- Fabrication of HBT devices on thin film SOI substrates.
- To optimize lateral SOI bipolar transistors and enable higher performance as simulations and theoretical studies predict.

**Strong points**

- Collaborative projects (UK) on bonded SOI SiGe HBTs - basic platform process established.
- SSOI technology proposed (UK) for a variety of device applications. Key features of the technology are the inclusion of a buried silicide layer above the buried oxide layer for the reduction of collector resistance, and the inclusion of a buried silicide groundplane (GP) below the buried oxide layer for crosstalk suppression.
- CLSEG process established and first lateral SiGe HBT reported (UK).
- First self-aligned SOI SiGeC HBT structure reported (France).

**Weak points**

- Lack of continuity and funding
- Industry not involved

**Conclusions and recommendations**

There is core expertise and competence distributed across a number of universities with an established platform technology to realise SOI-HBT, including the incorporation of buried silicide. Some novel solutions to issues such as buried ground planes for crosstalk, mitigation of self-heating with thermal vias, have been demonstrated. Some of the solutions are relatively expensive but the work is ready for exploitation if niche, value-added applications can be identified.

- Further improve of SOI base material for bipolar properties (high minority carrier lifetime).
- Development of high-performance and low-cost RF and analog/mixed-signal solutions.



#### 4.4.- SOI MEMS

##### **Comments**

One of the X-FAB standard technologies is a thick-SOI-wafer based surface micro machining technology for inertial sensors.

##### **Strong Points**

Leading edge technology.

##### **Weaknesses**

No international standards regarding long term reliability,  
No european project on NEMs (today)

##### **European Groups**

X-FAB is partner in several international projects, which are funded by the EU

LETI: Significant contributor

EPFL: Significant contributor

CSEM: Significant contributor

Colibrys: Significant contributor

Tronics: Significant contributor

##### **Conclusions and recommendations**

X-FAB's SOI technologies for MEMS applications have been developed for high volume applications in the automotive, industrial, aerospace and medical industries. First level of design kit is available.

#### 4.5.- OPTICAL SOI-WAVEGUIDES

##### **Comments**

In Silicon circuits, high refractive-index-contrast waveguides with a cross-section of the order of the wavelength squared are used to make passive or active devices. The core of the waveguide is Silicon while the cladding is either a dielectric (such as silica) or air. The waveguide can be a conventional waveguide based on guiding by total internal reflection or a photonic crystal waveguide based on guiding by Bragg diffraction.

##### **Strong Points**

Compatibility with the CMOS fabrication process

##### **Weaknesses**

Strong demands on fabrication accuracy.

Cost

##### **European Groups**

Leadership: IMEC

Contributors: CEA,VTT, Technical Danish University of Technology COM

##### **Conclusions and recommendations**

In a couple of years, Silicon-on-Insulator has become a major platform for photonic integrated circuits. Three European projects have a particularly interest in waveguide devices: European Network of Excellence FP6-ePIXnet, the European research project on on-chip optical interconnect FP6-PICMOS and the European Space Agency project on Multi Gigabit Optical Backplane Interconnections. The field is characterized by a strong competition around the world. Cost-reduction strategies are in progress to make this concept development viable



#### 4.6.- 3-DIMENSIONAL INTEGRATION

##### Comments

Many industry observers have questioned the economic viability of the next wafer diameter increase (450 mm), and suggested that a different source of increasing wafer fab productivity should be sought. These suggestions usually involve novel substrates and new circuit approaches. Novel substrates are thought of as large area, low cost, probably non-crystalline materials used as strata for single-crystal silicon. New circuit approaches include 3-D circuits and multi-valued logic, consistent with SOI wafers, or perhaps, radical approaches to 3-D circuitry. The widespread implementation of any of these alternatives to expand and/or replace silicon would be a major task for the industry, requiring an entire hierarchy of paradigms to be discarded and replaced with new ones.

##### Strong Points

##### Weak Points

Implementing new manufacturing technologies usually results in a decrease in productivity, at least in the early stages of implementation.

##### European Groups

STMicroelectronics, France

Infineon Technologies, Germany

##### Conclusions and recommendations

- 3-D circuits and multi-valued logic, and radical approaches to 3-D circuitry consistent with SOI wafers mean a huge challenge for the designers.
- The success of this approach could produce a reduction of the total cost, increasing the silicon yield.
- Few European groups are working on this area. More efforts should be dedicated to explore the possibilities of 3D integration.

#### 4.7. Novel devices

##### 4.7.1. Resonant Tunneling Diodes

##### Comments

The silicon resonant tunneling diode, compatible with the traditional mainstream microelectronics technology and circuitry, seems to be one of the most promising quantum-mechanical device for the post CMOS nanoelectronics era. The SOI technology offers a capability for integration of silicon-based resonant tunneling devices with conventional CMOS, this way helping CMOS technology in extending its march down Moore's Law. But not only "More Moore" way. Owing to its inheritable speed, multistability and increased functionality the resonant tunneling based architecture can help in realization of the "More than Moore" strategy to build qualitatively new electronics, as defined by the European Nanoelectronics Initiative Advisory Council (ENIAC).

Although, as one may conclude from the literature, the research on the Si/SiO<sub>2</sub> heterojunction resonant tunneling diodes seems to be still in the beginning stage, it may be revealed quite soon that the silicon resonant tunneling devices are ready for implementation and integration in the conventional circuits. European R&D groups and microelectronics industry should be prepared for this possibility.



### Strong Points

- European university groups collaborating within a framework of 6FP NoE SINANO have developed simulation tools enabling self-consistent calculations of the ultrathin double gate MOS structure with including energy quantization in both the conduction and valence band and the resonant tunneling for both electrons and holes.
- European microelectronics industry centres possess technology enabling fabrication of DG MOS structures with ultrathin silicon and silicon dioxide layers.

### Weak Points

- Lack of experimental works on resonant tunnelling in the double gate SOI structures, probably due to the difficulty for the university groups to get access to the ultrathin silicon double gate technology with separated gates. This makes impossible verification of theoretical models.

### European Groups

Warsaw University of Technology, Poland

Swiss Federal Institute of Technology,

Technical University of Vienna, Austria

Fraunhofer Institute of Integrated Systems and Device Technology, Germany

Chalmers, Göteborg, Sweden

VTT Technologies, Finland

### Conclusions and recommendations

- Resonant tunneling in the  $\text{SiO}_2/\text{Si}/\text{SiO}_2$  system needs more experimental confirmation.
- Resonant tunneling in the  $\text{SiO}_2/\text{Si}/\text{SiO}_2$  structures should be one of the strategic topics for the European nanoelectronics R&D groups, both in theory and technology.
- More collaboration between theoretical - simulation groups and industrial partners with a ultrathin double gate SOI technology is highly recommended.

## 4.8.- OPERATION AT HIGH TEMPERATURES OF SOI DEVICES

### Comments

It is demonstrated that: (a) the rise in free carrier charge densities with temperature results in an increased effective substrate capacitance as compared to that determined from the depletion approximation; (b) a correction to account for the inversion layer broadening, caused by lowering the surface electric field in a weak inversion region with temperature, must be introduced into the classical expression for the subthreshold slope.

It is also demonstrated that at high temperatures (above 100-2000 C depending on the Si film thickness and drain voltage) off-state current in SOI MOSFETs is due to the diffusion mechanism. A diffusion model for the high-temperature off-state current in SOI MOSFETs, which is based on the analysis of the potential and carrier concentration distributions in the Si film, has been developed. This model predicts a strong nonlinear dependence of the high temperature off-state current on the Si film thickness. A strong decrease in the high-temperature off-state current and improvement in on-to-off current ratio is expected to be for thin films and double-gate regime due. The proposed diffusion model allows one to explain all trends of the high-temperature off-state current behavior in EM SOI MOSFETs (namely, temperature and



silicon film thickness dependencies, channel length and drain voltage dependencies, back-gate biasing effect).

At sufficiently high temperatures and low drain voltages, the similar behavior of the offstate current is expected to be in EM and AM SOI MOSFETs. The high-temperature off-state characteristics of relatively short-channel ( $L < L_{diff}$ ) devices appear to be predictable without knowledge of the carrier lifetime or diffusion length.

#### **Strong Points**

Main physical processes responsible for high-temperature behavior of SOI MOSFETs are now clear.

#### **Weak Points**

C-continuous model for high temperature operated AM SOI pMOSFETs is not now developed, that results in difficulties in calculation of analog integrated circuits.

#### **European Groups**

UCL, Belgium  
Cissoid, Belgium  
ISP, Ukraine  
URV, Spain

#### **Conclusions and recommendations**

- Physical models, depicted high-temperature behaviour of SOI MOSFETs, was developed by European scientific groups
- Development of circuit models (C-continuous) for high temperature operated AM SOI pMOSFETs for long and short channels is necessary.
- Study of the effects of new buried oxides ( $\text{Si}_3\text{N}_4$ ) and optimization of device parameters such as breakdown voltage.



## **CHAPTER v. Devices. Simulation and modelling.**

### **5.1.- Process and Technology Simulation**

#### **Comments**

Process and technology simulation is important for understanding and optimizing transistor fabrication, pushing the limits of scaling traditional planar devices, and evaluating process issues in alternative device architectures. The fabrication of devices is simulated by dealing with a set of processes that reproduce the real chemical processes and give an idea of the geometrical structures obtained and its features in terms of doping profile and geometrical characteristics of the layers of different materials.

Simulators can be 1, 2 or 3-dimensional. The output of process simulation can be then used as an input for device simulations. In this way, different process options can be compared by analyzing their effect on the overall device performances.

With current commercial tools, complete process flows can be simulated, including implantation, deposition, etch, diffusion and oxidation of 3D structures. Specific 3D process effects, such as LOCOS and STI corners, can also be studied. To do so, efficient automatic mesh generators are used to facilitate the simulation. Finite elements algorithms among others are developed to deal with 1D-2D-3D geometries and efficient moving-boundary simulations.

More or less all the commercial tools include the possibility of simulating SOI devices since the differences with respect to the conventional devices are marginal. In fact, apart from the initial substrate of SOI wafers used to fabricate both FD or PD SOI devices, the processes involved in the fabrication are similar to non-SOI devices.

#### **European Position on the field**

There are research groups in Europe related to process simulations, however the commercial tools available for the industry come from very few companies, mainly located in the U.S.

The European TCAD company Integrated Systems Engineering AG has been recently acquired by the U.S. company Synopsys. A leading position in the field has been thus endangered.

#### **European Groups**

Technische Universität Wien, Austria

ETH, Zurich, Switzerland

STMicroelectronics, France

LPM - INSA de Lyon, France

CEA-DRT-LETI/DTS, France

Fraunhofer Institute of Integrated Systems and Device Technology, Germany

Infineon Technologies, Germany

#### **Strong Points**

- Knowledge related to almost all the processes involved in the fabrication of devices.
- Attempts to build tools.
- Experimental and fabrication facilities to develop model and to tune simulators.

#### **Weak Points**

- Not coordination between research and development centres.
- Efforts extremely scattered.
- Lack of reliable and complete tools.



- Lack of specific models for key SOI process steps including strained Silicon on SOI, SiGe on SOI and GOI substrates of possible interest for future devices.

### **Conclusions and recommendations**

The needs for process and technology modeling are driven by the reduction of feature size in scaling transistors and by the increasing number of new materials being considered to overcome scaling roadblocks. These not only cause higher demands on model accuracy but also require models for effects considered as second order effects in the previous node, or models of new materials, material properties, and doping techniques as well as the introduction of new simulation flows.

The efforts in this field seem to be scattered all along Europe and not coordinated at all. Therefore, a European coordination of the know-how, and most important the possibility to build a reliable and complete tool to be used by industrial partners in their development efforts would be a desirable goal, although hard to achieve also in light of the recent loss of control on one of the European leaders in the field (ISE has been bought by Synopsys).

The following issues have to be taken into account in order to improve the models and the accuracy of the simulations:

- High-k dielectrics and gate materials (material properties, interfaces, impurity diffusion).
- Ultra-shallow junction formation, which starts from very low energy implant and especially focuses on the thermal annealing and diffusion of dopants.
- Enhancement of models for Si based materials, including stress/strain and including flash/laser anneals and solid phase epitaxy.
- Topography modeling (deposition homogeneity).
- Planarization (cell-level CMP chip-level including dummy placement optimization, padwear and conditioning disc modeling, physics-based optimizations of rates, uniformity, and defect reduction).
- Surfaces (physics based feature scale models, integration of feature-scale simulation with equipment).
- Plasma models.
- The modeling of stress and strain and their influence on diffusion and activation has become vital, especially for strained silicon, SiGe, and for SOI structures.

## **5.2.- Device Simulation**

### **Comments**

Device simulators are used to perform scaling studies, technology optimization and to help to understand the experimental results obtained in new devices.

Commercial simulation tools are designed mainly for developing purposes in an industrial environment. With optimized accuracy/simulation-time rates, commercial simulators are useful for studies based on well established models and geometries. However, these tools usually lack the capability to correctly model non-conventional structures (GAA, FinFET, FD SOI) and the strong non-equilibrium transport effects taking place in decananometric devices.

Research simulation tools are used at universities and R&D departments to study new geometries, new effects and more accurate physical models with no restrictions on the computation time. Models and tools have been developed to deal with the modeling issues related to SOI structures and non-conventional materials (high-k, strained channels).

Many modeling approaches are possible:

- Drift-Diffusion/ Hydrodynamic (mainly implemented in commercial simulators), that have the advantage of robustness, are easy to use and require a very short computing time. However those tools, when applied to non- conventional architectures and decananometric channels, fail under many aspects: 1) difficult modeling of quantization effects in non-conventional structures (e.g. thin SOI films) 2) quantization effects on the transport (subband splitting, ...) cannot be properly taken into account, 3) the simplification introduced in the Boltzmann-Transport-Equation (BTE) in order to obtain those models, strongly reduce their applicability to quasi-ballistic transport .
- Ballistic transport simulation tools, based on the quasi-2D, fully 2D or quasi-3D solution of the Schrödinger equation. These tools properly account for quantization effect, including their influence on the transport (subband splitting, ...). Furthermore, in some cases, also quantum coherence along the transport direction and source-to-drain tunneling can be taken into account. However, these tools neglect scattering, that has been demonstrated to be important even in very short channel devices.
- Non-Equilibrium-Green-Functions (NEGF), include scattering in full-quantum simulations. So far only very simple scattering mechanisms have been included in some tools. Many tools referred as NEGF do not include scattering, but use the NEGF formalism to solve ballistic transport.
- Monte-Carlo simulators. They provide a full solution of the BTE and are thus adequate to simulated quasi-ballistic and non-equilibrium transport in very short channel devices. All the relevant scattering mechanism can be included. The effects of quantization on the charge distribution and on transport can be included in two ways: 1) by introducing quantum corrections to the potential in conventional semi-classical simulators, 2) by using the Monte-Carlo method to link together the subbands in different sections of the MOSFET (Multi-subband Monte-Carlo). In the first case, only the effects of quantization on the charge distribution can be taken into account, whereas the effects on transport can be taken into account only empirically (for example introducing surface roughness scattering models related to the vertical field, in order to reproduce the mobility of the inversion layer). In the second case, subband splitting and other effects related to quantization are taken into account in a natural way. Furthermore, in these tools the scattering rates are calculated accordingly with the theory of the 2D electron gas, and scattering mechanisms relevant in non-conventional structures (SO phonons, silicon film thickness fluctuation) can be included in a straightforward way.

Of course, other tools have been developed to study particular effects, e.g. mobility calculation based on the Momentum-Relaxation-Time approximation, the tools for the calculation of the tunnelling current across the dielectric.

### **European Position on the field**

Considering commercial device simulators, the key companies are in the U.S. The European TCAD company ISE has been recently acquired by the U.S. company Synopsys.

In the field of research device simulators, key groups in the world are in the U.S (Universities of Stanford, Urbana-Champaign, Arizona, Purdue, Florida, IBM) but European groups are not mere followers and have provided many original contributions to the field, demonstrated by a large number of papers in international journal and conferences in the field. The European position appears especially strong in the field of Monte Carlo simulators, with many groups having the capability to develop complete and advanced codes at the state of the art, if not better than those available in the US and Japan. Presently Monte Carlo techniques are considered as extremely promising for detailed analysis of deca-nanometric devices.



### **European Groups**

ISE Integrated Systems Engineering, Zurich (Switzerland)  
Technische Universität Wien (Austria)  
University of Glasgow (UK)  
University of Granada (Spain)  
University of Udine (Italy)  
University of Salamanca (Spain)

### **Strong Points**

Commercial simulators

- Well established models.
- Friendly Human-Machine interface.
- Fast convergence codes.
- Quantum effects for SOI included in most cases (only effects on charge concentration, not on transport).

Research level simulators

- Full custom physical models.
- “Exotic” device capability.
- New XOI and SOX material capabilities have been developed or under development.
- Benchmarking of the tools developed by the European groups is under way (through the Network of Excellence SINANO).
- Strong position in the field of Monte Carlo simulation.

### **Weak Points**

Commercial simulators

- Poor control on model definition.
- Lack of specific models for FD thin-film SOI, especially with regard to mobility and transport.
- Transport models not accurate for sub-100nm channels (full solution of the BTE is required).

Research level simulators

- Ultra thin layer transport model under development but not fully ready and calibrated yet.
- Available experimental data on basic transport properties is still very limited although efforts have been undertaken in the framework of the SINANO network of excellence.
- Some approaches are time consuming. A generalized effort to improve computational efficiency should be undertaken.
- Unfriendly Human-Machine interface.

### **Conclusions and recommendations**

Device models and numerical methods have to be developed to perform scaling studies and technology optimization. The key requirement to deal with these challenges is predictive simulation of materials, processes, and device behavior including reliability. Specific simulation tools have to be developed to take into account specific SOI characteristics and phenomena.

Significant progress has been recently done by the scientific community to understand mobility in UT silicon films for advanced CMOS devices. Models based on the scattering and transport theory of the 2D electron gas represent valuable calibrated tools to interpret effective mobility. Ensemble Monte-Carlo, and in particular Multi-subband Monte-Carlo, with physically based models for the most relevant scattering



mechanism in SOI devices represent valuable tools to compute the drain current, which go well beyond the simple calculation of the drain current in the ballistic limit.

Though the important presence of modeling works performed by European groups in the international literature referring to the study of SOI devices, the importance of this field for the development of the SOI roadmap requires to keep the effort by European researchers in order to not losing the advantage with respect to American and Asian groups, which devoted a very important activity to the modeling of experimental transistors in the last years. In particular, special attention must be paid to the highest-level research tools (ensemble device Monte Carlo simulators and in particular in the Multi-Subband form), since due to their features they are of great importance for both a full comprehension of the device physics (both for “conventional” and advanced transistors) and the development and optimization of SOI technologies.

Adapting the existing models or developing new ones that would be physically sound according to quantization of the channel and quasi-ballistic transport proper of ultra-scaled SOI transistors should be the primary tasks in the next few years, together with the comparison with experimental measurements for second-order magnitudes, which is necessary to assure the predicting capabilities of the device models. These tools should be extensively used to understand all the relevant aspects of carrier transport in scaled SOI devices, and to steer the development of simplified models that are both physically accurate and predictive. Strategic agreements should be promoted to foster the use of these tools inside the industry or in cooperation with the industry to address specific technology analysis and optimization problems and to transfer the acquired know-how toward companies specialized in TCAD development.

Other points that need to be addressed are:

- So far the efforts have been mainly devoted to modelling the static device characteristics (e.g. mobility and drain current). The aspects related to the RF performances, and in particular the comparison between the different device architecture is still at a preliminary status.
- Accurate modelling of high-frequency noise is one of the critical issues to guarantee the success of future nanoscale SOI transistors.
- Accurate predictive models for new materials (strained silicon, germanium, gate stacks including high-k) should be further pursued.
- Ensemble Monte Carlo simulation of Partially-Depleted SOI transistors is still an open field. In this case, together with the previously mentioned know-how about the calculation of dynamic and noise parameters, a bipolar simulation is required in order to take into account the contribution of the substrate (majority carriers) to the high-frequency performance of the transistor.
- Quantum-based and non-equilibrium (ballistic) device simulations are needed. Simulations must also be applicable to non conventional SOI devices (Finfets, GAA, Trigates, etc). Stress engineering must be enabled. Besides accuracy, efficiency is a key issue.
- Identify more in detail in which way simulation can most efficiently support the industrial development



## **CHAPTER VI. Reliability of SOI Devices and Circuits.**

### **6.1.- Wafer-Level Reliability**

#### **Comments**

Bulk material quality has been historically controlled by bulk gettering mechanisms. As the buried oxide is an effective diffusion barrier for many contaminants (Fe, Ni, Mg, Cr, Va, but not Cu) this technique is not effective in SOI. Alternative contaminant controls (clean processing, lateral gettering, etc) are crucial to maintain controlled carrier lifetime and good gate-oxide integrity.

Therefore, gettering techniques are ineffective for most metal contaminants, as the buried oxide provides an effective barrier, and the distances for lateral gettering is too large in view of scattering due to oxide interfaces. Bulk processes and equipment are often not adequate to control the contaminant level sufficiently low in view of the small effective silicon volume involved.

#### **European Position**

Europe has built a strong position in the application of SOI both in main-stream (AMD Dresden, Crolles alliance between ST, Freescale, and Philips) and in certain niche-applications, such as power-electronics, high-voltage electronics, and automotive applications. Naturally, numerous obstacles have to be solved in material fabrication and insurance of reliability of the products.

#### **Strong Points**

Extensive experience has been built with high-voltage and power circuitry, which is extremely sensitive to generation centers due to the large depletion zones involved. The presence of strong utilization and several equipment manufacturers in Europe could lead to a powerful alliance in combating contamination levels in SOI.

#### **Weak Points**

Currently the pockets of knowledge are poorly coordinated; hardly any concerted industry-wide effort is taking place. A standardization effort under control of an independent university may be useful to bring knowledge together and establish a "best practices" approach to equipment and process steps for minimizing contaminants.

#### **European Groups**

SOISIC Grenoble, France  
SOITEC Grenoble, France  
LETI-CEA, France

#### **Conclusions and recommendations**

- SOI unique defects, which lead to time dependent failure, have to be minimized to acceptable levels.
- Additional work on clean processing and improved gettering techniques would be useful.
- The following measures should be considered when characterizing the wafer-level reliability: Defect density ( $<0.1$  defects/cm<sup>2</sup>) across wafer, wafer-to-wafer, and lot-to-lot.
- Intra-wafer and inter-wafer variations produced by Chemical-mechanical polishing (CMP) need consideration on all material properties.
- Extensive knowledge on generation/recombination centres in SOI has been gathered through specific applications.



- Working for demanding automotive specifications (low ppm, “zero defects”) has honed the techniques to unprecedented levels.
- A further integration of European activities in terms of contaminant control and characterization methods through joint projects is necessary.
- A division of tasks between universities (mid- and long-term research, characterization methods) and industry (application-oriented improvement methodologies) is recommended.

## 6.2.- Electro Static Discharge (ESD)

### Comments

ESD protection ranges from designing protection circuits/devices against human handling (human body model [HBM]), machine discharges (machine model [MM]) and charged chips being charged and discharged (charge device model [CDM]). In all ESD protection networks, the ESD device must protect the active circuits from these events. With the aggressive scaling of CMOS, SOI, and BiCMOS technologies, the constraints (area, capacitive loading and leakage currents to list a few) on the ESD protection circuits are making them more difficult to design and meet the Joint Electron Device Engineering Council (JEDEC), Electrical Overstress (EOS)/ESD, and other industry recognized specification requirements.

As the scaling of CMOS-based devices continues, the frequency of the I/O circuits and other circuits that need to communicate off-chip to other chips is increasing. Ideally, the ESD device area needs to scale at a similar rate as the rest of the circuits and the capacitive loading of the ESD device to be reduced proportionally to the increase in the I/O circuit speeds. As the technology scales, the ESD current that ESD devices must be able to handle without damage occurring remains constant; this drives the need for innovation in improving the effectiveness of ESD devices in each new technology generation to allow the ESD device area and capacitive loading to be scaled/reduced.

### Strong Points

Power-integrated circuits have been successfully protected.

### Weak Points

Little established knowledge on MEMS, sensors and actuators.

### European Groups

Philips  
ST, Crolles, France

### Conclusions and recommendations

Recommendations that ESD devices must fulfil:

- ESD devices with low on-resistance along with low capacitive loading (<100 fF) for RF applications.
- Low turn-on voltage ESD devices (<0.5 V).
- Low leakage (<1 pA) ESD devices for low power applications.
- Correlation of ESD design elements to final product and understanding of performance gaps.

Compact model-related needs and questions:

- High current ESD device models compatible with running on industry standard spice simulators with self-heating and breakdown models incorporated into the compact equivalent circuit.
- RF quality ESD device models for RF applications (diodes, silicided and nonsilicided MOSFETS).



## Conclusions

- Most protection schemes developed for bulk may not be compatible with SOI structures. Develop a new set of ESD protection algorithms and circuits as conventional (bulk) ESD designs cannot be copied over to SOI (much SOI-specific design is necessary).
- The protection elements that can be used for the ESD protection of SOI circuits are mainly diodes and transistors.
- Diode protection seems more attractive for ESD protection of SOI circuits. The lateral diode is the best way to create a uniform diode in the SOI technology and it has been used for ESD because of its high current capability, low capacitive loading, low turn-on voltage and its simplicity to design.

## 6.3.- Latch-Up

### Comments

Latchup can be classified into two generalized categories: internal and external. Internal latchup occurs when circuits are not connected to I/O pads, whereas external latchup occurs when circuits or injection sources are connected to pads. With the aggressive scaling of CMOS, SOI, and BICMOS technologies, the ground rules are being reduced to allow greater numbers of transistors in a given die size. The reduction in the ground rules leads to smaller N+(PWELL)/P+(NWELL) spacing, which in turn increases the parasitic NPN and PNP betas, lowering the trigger currents/voltages and the holding voltage. With the introduction of triple well bulk CMOS technologies, new NPNs and PNPs are formed that will need to be considered beyond the classical NPNs and PNPs formed in a dual well bulk CMOS technology.

### Strong Points

Power-integrated circuits have been successfully protected

### Weak Points

Little established knowledge on MEMS, sensors and actuators

### European Groups

Philips

### Conclusions and recommendations

- Development of latchup device simulators with improved convergence and with breakdown and temperature models turned on.
- Design of effective guarding designs in I/O circuits.
- Reduced NWELL and PWELL sheet resistances for improvements in trigger currents while minimizing junction area capacitances and maintaining low junction area leakages for low power applications.
- Increased shallow trench isolation (STI) depths for reduction in parasitic betas.
- Development of RF quality parasitic NPN and PNP models for accurate transient latchup simulations.
- Improved extraction tools/algorithms to extract only the most important parasitic latchup structures.



## 6.4.- Electro-migration (EM)

### Comments

The increasing number of devices packed on the same semiconductor area is resulting in reduced interconnect geometries that are susceptible to increased metal migration and electromigration risks. Interfacial delamination is a continuing concern as the number of interfaces within the package increases with complexity.

Extensive EM checking is needed in circuit design and synthesis as well as place and route. Design tools need to be able to recognize high frequency nodes, place desired loads together, and do tight routing.

Stress migration of Cu vias and lines is one of the most critical concerns.

It has been demonstrated the current and temperature dependence of the EM phenomena.

### Strong Points

Effective methods needed for power-semiconductors implemented.

### European Groups

Philips

### Conclusions and recommendations

This topic provides a new challenge for thermal and mechanical device simulators, which is currently not well covered. Electromigration should have priority on those tools that simulate failure mechanisms.

Topics to be considered:

- Physics of mass transport and EM: diffusion mechanism (surface, lattice, grain boundary diffusion), current and temperature dependence, controlling a dominant diffusion mechanism (failure mode).
- Different resistance change vs. time characteristics under EM or thermal stress: spikes, gradual increase, abrupt failures during aging.
- Scaling of EM to smaller line sizes.
- Effect of ambient gases during EM testing (e.g., air vs. nitrogen).
- Interaction between EM and stress migration

## 6.5.- Radiation Effects

### Comments

SOI technology was firstly used for radiation-hardened space and military applications. The advantages of SOI technology arise from the fact that the active devices are built on top of an insulating layer. However, the buried oxide also introduces an additional source for radiation-induced charge trapping. Moreover, the total dose response of SOI devices is more complex than for bulk-silicon devices due to the insulating layer.

Process techniques that reduce the net amount of radiation-induced positive charge trapped in the buried oxide and device design techniques (such as the Body Under Source Field Effect Transistor (BUSFET)) that mitigate the effects of trapped charge in the buried oxide have been developed to harden SOI devices to bulk-silicon device levels. Preliminary measurements on narrow FinFET transistors show intrinsic radiation hardness. This is an extraordinary asset for promoting the commercialization of these type of circuits.

### Strong Points

Importance of the European aerospace industry.



### **Weak Points**

Little public domain work in this field in Europe.

### **European Groups**

Philips

### **Conclusions and recommendations**

This field could be crucial for the newly extended space activity of the European Union. Reliance on US technology could be detrimental for independent defense projects. Work on FinFETs should be encouraged.

## **6.6.- Mechanical Effects: Strain, thermal cycling**

### **Comments**

Mechanical stresses introduced by the increasing mass of passive solutions or the complexity of active solutions must be evaluated over the product's lifetime. Since SOI may not be as efficient at heat dissipation through the die because of the buried oxide—even with the lower power devices offered by SOI—intra-die thermal non-uniformity or “hot spots” may increase. Packaging is also an important issue when dealing with mechanical and thermal stress.

Mechanical stresses:

- Intrinsic stress (created during deposition)
- Thermo-mechanical (thermal expansion coefficient)

Mechanical Stability:

- Effect of thermal cycling on interface stability

### **Strong Points**

Extensive experience gained from volume production of power electronics

### **Weak Points**

There is currently no European effort to understand and model the thermo-mechanical effects on the reliability of SOI devices.

### **European Position**

The extensive knowledge gained through manufacturing of MEMS based on thermal and mechanical effects may help European institutions to gain an advantage in this field.

### **European Groups**

Philips

### **Conclusions and recommendations**

The area of mechanical fatigue on a micro-mechanical scale is poorly understood and will require further studies. Extensive work on this reliability issue is needed in terms of understanding and prevention of catastrophic failures.

It is necessary a deeper knowledge of thermo-mechanical stress effects (stress voiding, etc.):

- Mechanical stress effects on failure modes and mechanisms.
- Impact of stress on Electro-Migration (EM is done in compression, while real world is tensile).
- Degradation of interfacial adhesion over time.
- Impact of many operating thermal cycles (joule heating) on reliability.



- Ability of bumps to withstand thermal and mechanical stresses while providing sufficient current carrying capability. Solder joints fracture at 1<sup>st</sup> and 2<sup>nd</sup> level interconnects.
- Impact of increasing Coefficient of Thermal Expansion (CTE) mismatch between low- $\kappa$ , silicon and organic packages.

### 6.7.- Application-specific tests

#### Comments

A careful selection of acceleration factors is necessary. Philips made good experiences with voltage-, temperature-, and frequency acceleration. Many micro-mechanical devices suffer from stiction and unpredictable degradation of gliding surfaces. It would be very useful the development of simulation tools for concurrent optimization of circuit performance and reliability.

#### Weak Points

There is currently no European effort to develop application-specific tests to understand and model the reliability of SOI devices.

#### European Groups

Philips

#### Conclusions and recommendations

Life-testing should cover a representative fraction of the device lifetime, but no reasonable acceleration models have been established this far.

Tools to simulate electromigration, thermal-mechanical stress and process induced charging could save time in process production. Soft error detection and correction at chip and system level, including random logic faults.

### 6.8.- Novel Materials. Novel failure mechanisms.

#### Comments

Progressing towards smaller geometries requires novel materials to keep parasitic elements at bay in integrated circuits. Copper is needed for lower wiring resistance, low- $\kappa$  dielectrics are required to minimize timing delays, high- $\kappa$  gate dielectrics are required for good channel control while keeping tunneling currents at bay.

Scaling brings about new issues and concerns that have to be faced with integrated circuits based on SOI. Similarly, the increased complexity and performance requirements for packaging these products act as an exponential multiplier for many of the failure mechanisms besides introducing new ones. The more localized heating through dissipation and thermal isolation provides new challenges for SOI ICs. The lack of models, knowledge, and acceleration mechanisms lead to poor predictability of the reliability of SOI circuits.

Concerning to new materials a wide variety of issues related to their reliability have to be considered:

#### High- $\kappa$ Gate Dielectrics

Dielectric breakdown characteristics (hard and soft breakdown).

Influence of charge trapping and NBTI on threshold voltage stability.

Stability and number of fixed charges.

#### Metal Gate

Impact of metal-ion drift and/or diffusion on gate dielectric reliability.

Work function control and stability.



Metal susceptibility to oxidation.

Thermo-mechanical issues due to large thermal expansion mismatch.

Impact of implantation.

#### Copper/Low- $\kappa$ Interconnects

Cu vias and lines electromigration performance. Thermal-mechanical stability of the interfaces between metals, barriers and interlevel dielectrics and resulting line-to-line leakage.

Time Dependent Dielectric Breakdown (TDDB) of the Cu/low- $\kappa$  system.

Reliability impact of lower thermal conductivity of low- $\kappa$  dielectric.

Reliability issues due to the porous nature of the low- $\kappa$  dielectrics and moisture.

Reliability impact of the lower mechanical strength in the Cu/low- $\kappa$  system, including the impact of packaging.

#### **Strong Points**

In international comparison all players are quite on the same level, several international companies are seeking pre-competitive alliances to spread the risk.

The European MEMS field is very active through numerous start-up companies and a good network.

#### **Weak Points**

The European efforts seem poorly aligned and may lack the critical mass. Especially for SOI it may be advisable to establish a network to divide the tasks and strive for maximum efficiencies.

#### **European Position**

Europe has several strong research centres in this field, such as the Crolles alliance, Infineon, IMEC, LETI. The reliability of such materials will only be established through the industrialization of the materials.

#### **Conclusions and recommendations**

Multiple material changes are projected by 2008 or so (high- $\kappa$  gate dielectric, metal gate electrodes, strained Si, nickel silicide, etc). Near mid-gap metal gate electrodes will be desirable to set the threshold voltage for UTB SOI. Assuring the reliability and implementing into manufacturing all these new materials, processes, and structural changes in a relatively short period of time will be a difficult challenge.

Although subject to intense study for bulk processes, there is little known about the reliability of these new materials in the somewhat different application on SOI. Specifically the larger thermal gradients and more localized dissipation bring new challenges to these materials.

- Coordination with work going on in bulk materials.
- Establish network to pay attention to SOI-specific requirements and challenges.
- Extensive collaboration between research centres (universities: modelling and understanding) and industry (providing critical statistical information) is recommended and requires some coordination.
- Integration of some leading MEMS players in this field is strongly recommended.



## **CHAPTER VII. Physics. Non-Conventional Device Physics.**

### **7.1.- Transport enhanced FETs**

#### **Comments**

Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs is a major challenge to be faced in a near future. Advanced non-classical CMOS (e.g., multiple-gate, ultra-thin body [UTB] MOSFETs) with lightly doped body will be needed to effectively scale MOSFETs well under 20 nm gate length ( $L_g$ ).

For digital applications, the scaling challenges include controlling leakage currents and short-channel effects, increasing saturation current while reducing the power supply, control of device parameters (e.g., threshold voltage, leakage) across the chip and from chip to chip. For analog/mixed-signal/RF applications, the challenges additionally include sustaining linearity, low noise figure, power-added-efficiency, and transistor matching. The industry and academic communities are pursuing two avenues to meeting these challenges—new transistor structures and new materials. New transistor structures seek to improve the electrostatics of the MOSFET, provide a platform for introduction of new materials, and accommodate the integration needs of new materials. New materials include those used in the gate stack (high- $\kappa$  dielectric and electrode materials), those used in the conducting channel that have improved carrier transport properties, as well as new materials used in the source/drain regions with reduced resistance and carrier injection properties. Additionally, the combination of new device structures and new materials enables new operating principles that may provide new behavior and functionality beyond the constraints of bulk planar or classical CMOS.

Improvements in transistor drive current for improved circuit performance can be achieved by enhancing the average velocity of carriers in the channel. Approaches to enhancing transport include mechanically straining the channel layer to enhance carrier mobility and saturation velocity, and employing alternative channel materials such as silicon-germanium, germanium, or III-V compound semiconductors with electron and hole mobilities and carrier velocities higher than those in silicon. A judicious choice of crystal orientation and current transport direction may also provide transport enhancement. However, an important issue is how to fabricate transport enhanced channel layers (such as a strained Si layer) in several of the non-classical CMOS transistor structures. To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced carrier saturation velocity appears to be needed.

#### **Strong Points**

Fabrication facilities.

Advanced modelling tools for Si that can be easily extended to strained Si and Ge channels.

#### **Weak Points**

The origin of the mobility improvement in strained Si has not been fully clarified yet.

#### **European Groups**

VTT Technology, Finland

CEA-DRT-LETI/DTS, France

Fraunhofer Institute of Integrated Systems and Device Technology, Germany

Infineon Technologies, Germany

IMEC, Belgium



UCL, Belgium

### Conclusions and recommendations

- Increased funding of long term research.
- Study of the impact of quantum effects in UTB MOSFETs with body thickness under 10 nm.
- Identifying, selecting, and implementing novel interconnect schemes.
- Control of boron penetration from doped polysilicon gate electrode.
- Control of silicon loss at spacer etch and gate etch needs to be much tighter on thin SOI and SiGe wafers, where the total silicon thickness is 20-50 nm.
- Minimized depletion of dual-doped polysilicon electrodes.
- Explore the possibility to implement III-V device concepts on SOI.

### 7.2.-Metallic gate FETs

#### Comments

Metal gate electrodes are projected for 2008, in order to effectively prevent gate electrode depletion and hence allow acceptable scaling of the equivalent electrical oxide thickness in inversion. To set the threshold voltage correctly, the gate electrode work function needs to be near the silicon valence band for PMOSFETs and near the silicon conduction band for NMOSFETs. In fact, one electrode material with work function tunable within several hundred meV on either side of midgap is desirable. Due to the lightly doped and fully depleted channel, the threshold voltage control by the work function of the gate electrode, and the ultra-thin body, these SOI MOSFETs are considerably more scalable and develop more saturation drive current than comparable planar bulk MOSFETs

#### Strong Points

No poly depletion effects, no boron penetration, very low resistance and suppressed remote charge scattering.

#### Weak Points

More experimental and theoretical work has to be done in the field of metal gate technology. Few European groups are working in this field.

#### European Groups

IMEC

### Conclusions and recommendations

The use of metal gates will be mandatory to overcome poly-Si drawbacks. Much experimental work should be done in this topic since different questions remain unsolved (e.g.: Metal gate still suffer from the inadequate tuning of the workfunctions for threshold voltage ( $V_{TH}$ ) definition of both n- and p-MOS).

- Europe is well behind US and Asia in this topic.

### 7.3.-Ultrathin body SOI FETs

#### Comments

A very thin transistor body is employed to ensure good electrostatic control of the channel by the gate in the "off" state. Typically, the ratio of the channel length to the channel thickness will be  $\geq 3$ . Hence an extremely thin (<4 nm) Si channel is required to scale CMOS to the 22 nm node. The use of a lightly doped or undoped body provides



immunity to  $V_T$  variations due to statistical dopant fluctuations, as well as enhanced carrier mobilities for higher transistor drive current. The localized and ultra-thin BOX FET is an UTB SOI-like FET in which a thin Si channel is locally isolated from the bulk-Si substrate by a thin (10–30 nm) buried dielectric layer. This structure combines the best features of the classical MOSFET (e.g., deep source/drain contact regions for low parasitic resistance) with the best features of SOI technology (improved electrostatics). The increased capacitive coupling between the source, drain, and channel with the conducting substrate through the ultra-thin BOX has the potential of reducing the speed of the device but also of improving the electrostatic integrity of the device. The former may be traded against the latter (by reducing the channel doping) that eventually leads to moderately improved speed for a constant  $I_{off}$ .

### **Strong Points**

Compatible with bulk technology since no significant changes in design are necessary. Experience and knowledge in the study of quantum effects in other MOS structures.

### **Weak Points**

The fabrication of UTB SOI FETs with uniform thickness below 10nm (even below 5nm) represents a major task that push the technology to their limits. Difficult to adjust threshold voltage since metal gates are necessary with undoped bodys.

### **European Groups**

CEA-DRT-LETI/DTS, France  
VTT Technology, Finland  
University of Granada, Spain

### **Conclusions and recommendations**

Ultra-thin body SOI FETs offer a promising way to improve CMOS performances beyond classical MOSFET capabilities because the improved electrostatics and low junction capacitance. We recommend exploring intensively several fabrication issues related with the control of the threshold voltage and silicon body thickness and defect density. Other major issue is the impact of quantum effects in UTB MOSFETs with body thickness under 10 nm.

Confined phonons could determine the transport properties of these UTB SOI FETs.

## **7.4.- Source and Drain Engineering**

### **Metallic S/D junctions & Non-overlapping S/D junctions**

#### **Comments**

The impact of source and drain (S/D) parasitic resistances has been identified as a roadblocks for the 45 nm technology node and below.

The basic idea to avoid S/D access resistance problems is to replace the doped S/D regions by metallic Schottky contacts, so at low  $V_{GS}$  the barrier from metal to semiconductor is high enough to avoid the injection of carriers into the channel, while at high  $V_{GS}$  the barrier is thinned down and it tends to become transparent to injected carriers. With this solution there is no need of ultra-shallow p-n junctions, and the problems associated to the tight constraints of dopant activation to achieve highly doped junctions and the need of steep lateral profiling are inherently solved.

The use of non-overlapping S/D junctions can be extremely interesting in ultrascaled devices. Among the benefits provided by such S/D architecture, the most relevant are the minimization of the parasitic gate capacitance (which can be critical for very short



channels) and a reduced short channel effect and drain-induced barrier lowering. As main drawbacks, access resistances are increased and the output current is degraded.

### **Strong Points**

Significant top-quality results in the investigation of Schottky Barriers (SB)-MOSFETs. Coordinated efforts between the groups (SODAMOS and METAMOS European Projects).

Non-overlapped S/D produces a reduction of the parasitic gate capacitance. This fact is specially important for channels lengths in the nanometer range.

### **Weak Points**

High-frequency noise characterization of SB-MOSFETs is necessary. Need of accurate models to represent the high-frequency dynamic and noise performance of transistors.

### **European Groups**

IEMN (France)  
Université Catholique de Louvain (Belgium)  
University of Salamanca (Spain)  
Institute of Electron Technology (Poland)  
ST Microelectronics  
Philips Semiconductors

### **Conclusions and recommendations**

Metallic S/D junctions are a highly recommendable alternative to avoid the problems associated to elevated parasitic S/D resistances in ultrascaled devices. Europe holds a strong position in the field due to the coordinated effort of several groups. At the present moment this technology is still under development, so still more research at the academic and industrial level is needed in the short and mid terms to make it completely feasible for commercial applications. Strong efforts must be made to determine the possibilities of SB-MOSFETs for analog high-frequency applications.

The non-overlapped architecture has main advantages for overcoming short channel effects that arise when scaling down the MOSFET. They also present a very attractive scheme to build single electron transistors with standard silicon microelectronics processes and without electron beam lithography.

## **7.5. Double gate devices**

### **Comments**

The double gate SOI transistor is regarded as the best candidate for helping the CMOS process in continuing its evolution according the "More Moore" strategy, defined by the European Nanoelectronics Initiative Advisory Council (ENIAC).

Although the double gate SOI structure requires more advanced design and fabrication process, many examples of successful fabrication have been presented. The fabrication process can be fully compatible with the conventional one whereas the additional capabilities and beneficial features of the DG SOI transistor make it very attractive for practical implementation.

In dependence on the geometry (configuration of the transistor, semiconductor layer thickness, gate oxide thickness) the double gate FET can exhibit several beneficial features (compared to the single gate SOI transistor):

- Higher drain current and transconductance (especially in the volume inversion transistors).

- Increased immunity to short channel effects (especially for ultrathin semiconductor layers).
- A reduced subthreshold swing (in the FD transistors).
- Higher electron mobility (in the limited range of the semiconductor thickness).
- An increased functionality (adjustable threshold voltage, circuit logic functions) if the gates are controlled independently.

A variety of double-gate MOSFET structures have been proposed to improve engineering of the channel electrostatics and, in some cases, to provide independent control of two isolated gates for low-power and, perhaps, mixed-signal applications. Four typical double-gate structures are commonly described. First is the *sidewall conduction* structure. This is a double-gate transistor structure in which current flows horizontally (parallel to the plane of the substrate) between the source and drain, along opposite vertical channel surfaces. The width of the vertical silicon fin is narrow (smaller than the channel length) to provide adequate control of short-channel effects.

The second structure is the tied double-gate planar FET. In this structure, current flows horizontally (parallel to the plane of the substrate) between the source and drain along opposite horizontal channel surfaces. The top and bottom gate electrodes are deposited in the same step and are defined lithographically. The source/drain regions are typically self-aligned to the top gate electrode. The principal advantages of this structure reside in the simplicity of the process (closest to bulk planar process) and in the compactness of the layout (same as for bulk planar) as well as in its compatibility with bulk layout (no need for redesigning libraries). Also important is that the channel thickness is determined by epitaxy, rather than etching, and thus is very well controlled. The challenge resides in the doping of the poly in the bottom gate (shadowed by the channel), but this problem disappears automatically when switching to a metal-like gate electrode. Another challenge is in the fabrication process, particularly for those structures requiring alignment of the top and bottom gate electrodes.

The third structure is the independently switched double-gate (ground-plane) FET. This structure is similar to the planar tied double-gate FET, except that the top and bottom gate electrodes are electrically isolated to provide for independent biasing of the two gates. The top gate is typically used to switch the transistor "on" and "off" while the bottom gate is used for dynamic (or static)  $V_t$  adjustment. The principal advantage is in the very low  $I_{off}$  this structure offers. The disadvantage is in rather poor subthreshold behavior and in the relaxed layout. The fourth structure is the vertical transistor. In this case, current flows between the source and drain in the vertical direction (orthogonal to the plane of the substrate) along two or more vertical channel surfaces. The gate length, hence the channel length, is defined by the thickness of the single deposited gate layer, rather than by a lithographic step. The gate electrodes are electrically connected, and are vertically self-aligned with each other and with the diffused source/drain extension regions. The principal advantage with this structure is that the channel length is defined by epitaxy rather than by lithography (offering the potential of very short and well-controlled channel). The disadvantage is that this structure requires a challenging process and the layout is different from that for bulk transistors.

### Strong Points

- Many teams in Europe are engaged working on physics and simulation of the double gate SOI devices. Their knowledge and expertise fields are complementary, creating a very strong scientific community.
- Simulation of all issues concerning the double gate SOI structures (electrostatics, carrier concentration distribution, transport, current-voltage characteristics) is a subject of collaboration in the framework of SINANO NoE.



- European microelectronics centres have developed technology enabling fabrication of DG MOS transistors with ultrathin silicon and ultrathin silicon dioxide layers.

#### **Weak Points**

- There is a lack of experimental results related to the double gate devices. This difficulty to compare models and simulations makes impossible the verification of theoretical models.

#### **European Groups**

ENSERG, Grenoble, France

University of Bologna, Udine, and Pisa, Italy

University of Granada, and University of Salamanca, Spain

Warsaw University of Technology, Poland

UCL, Louvain-la-Neuve, Belgium

Swiss Federal Institute of Technology, Switzerland

Technical University of Vienna, Austria

Fabrication:

ST Microelectronics, Crolles, France

CEA-LETI, Grenoble, France

#### **Conclusions and recommendations**

- European groups are strong in the field of theory and simulation of the double gate SOI devices as well as there is knowledge and practical experience for implementation of this technology into the industry.
- More collaboration between universities and industry is strongly recommended in order to check simulators and models with experimental data.
- Misalignment of gates is an important technological challenge since it produces a reduction on the device performance.
- Develop circuit design using the independent signals applied to each gate to reduce the transistor count in logic circuits and to enhance the functionality of analog circuits.

### **7.6.- Multigate devices**

#### **Comments**

With scaling, difficulties arise with planar bulk MOSFETs because of high channel doping, inability to adequately control short channel effects, and others. The advanced CMOS technologies can be scaled more effectively. In fact, multiple-gate MOSFET scaling is superior to UTB FD MOSFET scaling, and hence the ultimate MOSFET is projected to be the multiple-gate device. Multiple-gate, ultra-thin body, fully depleted MOSFETs are more complex and more scalable, and are projected to be implemented in 2011 for high-performance logic.

#### **7.6.1.- FinFets**

#### **Comments**

The FinFET is a double-gate transistor structure in which current flows horizontally (parallel to the plane of the substrate) between the source and drain, along opposite vertical channel surfaces. The width of the vertical silicon fin is narrow (smaller than the channel length) to provide adequate control of short-channel effects. Recent studies have analyzed the response of FinFETs to dose irradiation.



### **Strong Points**

The principal advantage with this structure is the planar bulk-like layout and process. Higher drive current. Improved subthreshold slope. Improved short channel effect. Relatively easy process integration. Potential to push the limits of scaling beyond what is attainable with planar, single-gate MOS technology.

### **Weak Points**

The major challenge is with fabrication of thin fins that need to be a fraction ( $1/3$ – $1/2$ ) of the gate length thus requiring sub-lithographic techniques.

### **Conclusions and recommendations**

- One of the major challenges related with the fabrication of FinFETs is that the fins need to be a fraction ( $1/3$ – $1/2$ ) of the gate length thus requiring sub-lithographic techniques.
- Compact modelling is another important issue at the present stage of development of FinFET technology.
- Develop circuit design using the independent signals applied to each gate in Mu-FinFETs to reduce the transistor count in logic circuits and to enhance the functionality of analog circuits.

## **7.6.2.- Vertical transistors**

### **Comments**

The current flows between the source and drain in the vertical direction (orthogonal to the plane of the substrate) along two or more vertical channel surfaces.

The channel length is defined by the thickness of the single deposited gate layer, rather than by a lithographic step.

### **Strong Points**

The principal advantage is that this structure is that the channel length is defined by epitaxy rather than by lithography (possibility of very short and well-controlled channels).

Potential for 3D integration. Up to 30% gain in layout density.

### **Weak Points**

The disadvantage is this structure requires a challenging process and the layout is different from that for bulk transistors.

Difficulties in junction profiling and process integration. Increasing parasitic capacitance.

### **Conclusions and recommendations**

The vertical transistor offers the best scaling potential. We recommend focusing on process integration and layout design. Compact modelling and physical models are required to explore the capability of the vertical transistor at both the device and circuit levels.

### 7.6.3.- Gate-all-around and G4-FET FETs

#### Comments

In the N-gate MOSFET current flows horizontally (parallel to the plane of the substrate) between the source and drain along vertical channel surfaces, as well as one or more horizontal channel surfaces. The large number of gates provides for improved electrostatic control of the channel, so that the Si body thickness and width can be larger than for the ultra-thin-body SOI and double-gate FET structures, respectively.

#### Strong Points

The principal advantage of the structure resides in the relaxation of the needs on the thinness of the Si-body or the vertical fin. A thicker Si body is possible without degrading the device performance. The excellent electrostatic control of these devices will be very useful for sub-25nm gate lengths, in addition to enhanced transport properties.

#### Weak Points

Limited device width. Presence of corner effects. Sub-lithographic fin thicknesses are required. 3D simulations and models including quantum effects are necessary. 2D electron confinement produce a 1D density of states that has to be considered for accurate modeling and simulation.

#### European Groups

UCL, IMEC

#### Conclusions and recommendations

Multiple gate MOSFETs offer a very practical solution for relaxation of the thickness of Si-body. We recommend to explore N-gate FETs, especially fabrication problems, and modelling for projecting the maximum performances. More exploratory work should be done in order to fully understand these new structures and to exploit them for revolutionary circuits. The circuit design opportunities brought by separated gate devices should be carefully considered.

### 7.7.- Ballistic Transistors

#### Comments

As the gate length is scaled well below 20 nm, the fully depleted, lightly doped SOI-MOSFETs are likely to operate in a quasi-ballistic mode, with enhanced transport due to reduced scattering, and hence enhanced saturation current drive.

Improvements related to reduced scattering in short MOSFETs, are more evident in the case of low-doping UTB-DG SOI devices, than in bulk ones. In the latter case, ballistic effects are limited by a larger impact of surface roughness effects. In the case of UTB-DG MOSFETs, SOI phonons are dominant and there is no way to reduce their impact, other than changing the material properties or the operating temperature.

Self-consistent full-band Monte Carlo simulation represents the ideal tool to analyse the role of scattering in the channel and in the drain of MOSFETs with channel lengths below 100nm. MC analysis can handle the progressive transition from scattering-dominated transport to quasi-ballistic transport, that occurs as the channel length is scaled to values close to the carrier mean free path.

#### Strong Points

European groups have developed physically based simulators prepared to analyze the behaviour of devices with effective gate length below 25 nm.

Maximum drive current and speed.



### **Weak Points**

Lacking of experimental data to compare theoretical results.  
The scattering sources are very difficult to control.

### **European Groups**

University of Udine, Italy  
Universitat Autònoma de Barcelona, Spain

### **Conclusions and recommendations**

We should understand this phenomenon, by the use of physical models that account for scattering mechanisms and quantum mechanics, device simulations and if possible actual fabrication of devices. Compact models are needed for exploring the resulting performances at the circuit level. Also, the present gap between the results predicted by analytical models and rigorous simulations has to be bridged. Efforts have to be directed to address the issues that impede the ballistic transport, like reducing the channel scattering, improving the Si-SiO<sub>2</sub> interface and use of multiple gate structures. The use of different channel materials (strained-silicon or germanium), featuring higher injection velocity and lower scattering, is expected to enhance the on-current. The ballistic transistor offers the maximum performance; it must be considered at the ultimate scaling limits.

## **7.8.- High-k materials**

### **Comments**

It is projected that high-k gate dielectric will be required by 2008. However, to successfully integrate a high-k dielectric material into CMOS technology, its electrical device performance (carrier mobility, stability, reliability...) has to match that of SiO<sub>2</sub>. Another important challenge concerns the thermal device design of SOI transistors with metal electrodes and high-k insulators.

### **Strong Points**

High-k dielectrics provide a path for simultaneously controlling the gate leakage current and short-channel effects.

### **Weak Points**

Reduction of the electron mobility produced by phonons related with the high-k materials.

Leading activities in the high-k insulator field are developed in Japan (Toshiba, NEC, etc) and US (IBM and Universities).

### **European Groups**

IMEP, Grenoble, France

### **Conclusions and recommendations**

- Aggressive competition outside Europe.
- More research in metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization.
- Identification of p+ and n+ metals and their integration in a CMOS process are a challenge. It is also needed a thermal analysis of SOI transistors using high-k materials.
- Implementation of high-k gate stacks with metal gates in scaled devices (metal deposition, patterning, integration issues, characterization). Fundamental understanding of future gate stack materials and their impact on the electrical properties and reliability of scaled devices.



Thematic Network on Silicon on Insulator Technology, Devices and Circuits.  
[IST-1-506653-CA]

- Research on removal of high-k dielectric without loss of the underlying silicon, especially in the case of SOI or non planar devices.



## **CHAPTER VIII. Circuit Design**

### **8.1.- Transistor modeling for circuit simulators**

#### **Comments**

In order to link the improvement caused by device scaling and by the introduction of new device concepts (Fully-Depleted SOI, FinFET, GAA, ...) to the performance of the circuits built using these devices, accurate compact models for SOI devices, suitable for their implementation in circuit simulators such as SPICE, are required. These SPICE models may be able to handle specific SOI requirements:

- Fully Depleted and Partially Depleted channels
- Volume inversion in DG MOSFETs
- Possibility of floating body effects
- Single- and Double-Gate configurations
- High-k dielectric
- Si-Insulator interface
- Detailed quantum modeling
- Tunneling through the thin gate oxide
- Self-heating
- Quasi-ballistic transport in very short channel devices

Compact models for future SOI MOSFETs should model new effects correctly. Examples are mobility-enhanced channels and high- $\kappa$  gate leakage. Many devices have fully depleted channels, like FD SOI-CMOS, FinFET, Omega FET, dual gate FET, etc. This enables shorter channels, which means more ballistic effects. Moreover, two channels close to each other (10 nm) will have quantum mechanical interactions. This is important in multi-channel devices like FinFET and dual gate FET. Given the small dimensions, variability and statistics will be more prominent in this class of devices and should be also considered in their models for circuit simulators.

There are several research groups that have developed compact SOI MOSFET models addressing a subset of the above described requirements. A few SOI MOSFET models developed by European groups (LETI, STAG) are available in main commercial circuit simulators.

#### **Strong Points**

LETISOI and STAG are implemented in many commercial simulators. They are models for PD SOI MOSFETs. They are formulated in terms of the surface potentials.

#### **Weak Points**

Philips level 11 model extended with Penn University has been selected as the standard for nanoscaled MOSFETs by the modelling council but not extended to SOI yet. Philips is not known to collaborate with SOI experts.

The models LETISOI and STAG were not been extended to the nanoscale range of channel lengths. They are not valid for FD SOI MOSFETs.

Despite the work done by the European groups who developed LETI and STAG, models for PD SOI MOSFETs developed by Berkeley (BSIMSOI) or the University of Florida (UFSOI) have become more suitable for circuit simulation, because they were extended to the nanoscale range and also to FD SOI devices.

The main difficulties for Europe to become leader in the field of compact SOI MOSFET modeling are:

- Lack of coordination between groups.
- Efforts extremely scattered.
- Standard models such as Philips not always "open-source".



Less effort was done in Europe regarding compact modeling of FD SOI MOSFETs (practically only UCL worked on the modeling of this device). However, recently, several European groups have started to work on the development of compact models for multiple-gate SOI MOSFETs. For Europe, it would be desirable that these groups coordinate their efforts in order to achieve a kind of standard model for nanoscale multiple-gate SOI MOSFETs available in commercial circuit simulators.

### **European Groups**

The European groups who have developed compact models implemented in commercial circuit simulators are:

- 1) LETI (Laboratoire d'Electronique, de Technologie et d'Instrumentation), CEA-Grenoble (LETI model).
  - 2) Southampton University Microelectronics Centre, England (STAG model).
  - 3) SOISIC (Silicon on Insulator Systems and Integrated Circuits) GRENOBLE, France.
- Other European groups have been working on single- or multiple-gate SOI MOS compact modeling: UCL, URV, IEMN (regarding noise), University of Pisa, IMEP, CNRS in Marseilles.

### **European Position in the field**

Most of the key groups in the development of circuit simulation tools and compact models are based in the U.S. (Cadence, Synopsys, University of Berkeley, University of Florida). However, many European groups (CEA-LETI, Philips Research, Southampton University, SOISIC, EPFL, UCL, URV, University of Pisa, IMEP, CNRS in Marseilles) have developed their own compact models accounting for specific effects present in SOI devices. Some of them hold positions close to the lead, especially regarding multiple-gate SOI MOS devices.

### **Conclusions and recommendations**

Important compact modeling work has been carried in Europe; however, there has been a certain lack of continuation of the work started.

Regarding PD SOI MOSFET modelling, the LETISOI and STAG models are PD SOI MOSFET models implemented in many circuit simulators. Their weakness is that they were not validated for devices with less than 100 nm of channel length. It seems that there is no European group working on the development of a compact PD SOI MOSFET model for sub-100nm devices.

Regarding FD SOI MOSFET modeling, less work has been done in Europe. LETISOI and STAG were not extended to these devices. A model for FD SOI MOSFET was developed at UCL, but is not available in the main commercial circuit simulators, and was validated only down to 130 nm.

On the contrary, BSIMSOI and UFSOI models have been adapted to sub-100nm devices for PD and FD devices. In particular, UFSOI has shown to provide good accuracy for devices with a 70 nm channel length.

However, it is worth to mention that European contribution to compact modelling of double and multiple-gate SOI MOSFETs has become very strong in the last years, in the framework of the SINANO Network of Excellence. So far, there are practically no compact multiple-gate SOI MOSFET models available in commercial versions of circuit simulators. The UFDG model (developed by the University of Florida), although not yet available in circuit simulators, has been proven to accurately fit the numerically simulated characteristics of FinFETs down to a channel length of 100 nm.

European coordination of the know-how, and most important the possibility to build a tool complete and reliable enough to be used by industrial partners in the development efforts would be very desirable.

Points that need to be addressed by future compact models are:

- Proper modelling of series resistances in active devices.



- Non-quasi-static models.
- Harmonic distortion.
- Influences of statistic aspects on device parameters.
- Quasi-ballistic effects, to be analyzed and addressed in strict cooperation with device modeling groups.
- Quantum confinement in the Si film
- Concerning interconnects and integrated passives: need for On-chip inductance effects, frequency dependent resistance, hierarchical full chip RLC, inclusion of reliability aspects.

Given the new forefront position of Philips model, pan-European collaboration should be launched towards its extension to SOI. It depends on Philips openness.

## **8.2.- Digital Logic**

### **8.2.1.- High-speed (Microprocessor, Data Communications)**

#### **Comments**

For high-performance chips, the high subthreshold leakage current must be dealt with to keep chip static power dissipation within tolerable limits. One common approach is to fabricate more than one type of transistor on the chip. One is a high-performance, low  $V_T$  device, as well as other devices with higher  $V_T$  and larger EOT to reduce the leakage current. These alternate, lower leakage devices will have lower saturation drive current and hence poorer device performance (lower intrinsic switching frequency) than the high-performance devices. The high-performance device is used just in critical paths, and the low leakage devices are used everywhere else. Extensive use of the low leakage devices can significantly reduce the chip static power dissipation without seriously degrading chip performance.

Current circuit/architectural techniques to cut down static power dissipation include pass gates to cut off access to power/ground rails or other techniques to power down circuit blocks.

Hence, a realistic picture of scaled high performance ICs is that the static power dissipation will be controlled by utilizing more than one type of transistor and by utilizing device/design/architectural techniques.

#### **Strong Points**

Very strong know-how of SOI technology, devices and basic circuits. Potential exploitation of advanced SOI technologies (90nm, 65nm).

#### **Weak Points**

No/few SOI experience on big circuit design (e.g. microprocessors, SoC).

#### **European Groups**

CEA-Leti, France (M. Belleville): Contributor in digital circuit design, methodologies, Dynamic Threshold MOS (DTMOS)

STMicroelectronics, France (P. Flatresse): Contributor in libraries design and characterization methods.

Polito, Italy (M. Casu): Contributor in DTMOS for high-speed and libraries characterization methods.

#### **Conclusions and recommendations**

There is a gap in EU w.r.t. USA in high-speed digital circuit design (academia and industry) although the know-how is present in EU. It is highly desirable to grow and exploit it in SoC mixed-signal design, where general purpose and dedicated processors are integrated with analog and RF, targeting wireless telecommunications where EU



holds an outstanding position. EU researchers should also contribute to demonstrate the performance of advanced and alternative technologies (e.g. double gate, Finfet, multiple-gate SOI MOSFETs) on basic digital circuits for high-speed applications.

To sum up, we can conclude that the lack of EU driver has resulted in a lack of coordination so far. Given that the generic microprocessor market is occupied by Intel, IBM, AMD, Freescale..., and the DSP market by TI. Europe can penetrate the specialized microcontroller market (for industrial sectors, automotive...) as well as the embedded microprocessor segment (especially for telecom which require more and more computing power (mobile phones, xDSL...)).

### 8.2.2.- Low-power / Low-voltage

### 8.2.3.- Ultra Low-voltage

#### Comments

For low-power chips, the key goal is low power dissipation in order to enhance battery life, with a tradeoff of low performance compared to high-performance chips. This overall goal is attained through the use of transistors with low  $I_{ds,leak}$  as well as through the approaches utilized for high-performance logic: multiple transistors on chip and application of circuit and architectural techniques, including power management techniques to reduce chip leakage current in the standby mode.

#### Strong Points

The main advantages of SOI devices for ultra-low voltage operation are obtained with Fully Depleted (FD) SOI technology where European expertise is available.

#### Weak Points

Multi-threshold voltages limited in deep-submicron technologies.

#### European Groups

LETI, Marc Belleville Group STMicroelectronics

Polito, Italy (M. R. Casu): ULV design inPD-SOI

ISEP, France (A. Amara): Modeling, ULV SRAM memory design, ULVComputing

UCL, Belgium (D. Flandre): Ultra-low power digital blocks, SRAMs

CISSOID, Belgium (L. Demeus): Ultralow power design

#### Conclusions and recommendations

MTCMOS (Multi-Threshold CMOS) techniques are still difficult to implement in deep-submicron technologies because only 1 or 2 threshold voltage values are available, which is not enough in some digital designs, especially in designs that require a negative  $V_T$  for n-type and p-type transistors. SOI technology offers many advantages for tomorrow's Ultra-Low-Power driven applications. Some open issues such as noise immunity, delay penalty compensation based on innovative circuits and architectures need to be addressed by the research community in Europe. The results obtained in Japan demonstrate the strength of SOI technology for ultra-low voltage digital design. European groups have the required know-how in SOI technology and ultra-low voltage circuits design but up to now, the results that were obtained were not implemented in complex systems. Then, Europe is well behind other countries in a field with huge economic potential since battery and portable equipments are becoming ubiquitous.



### 8.3.-Memories

#### Comments

In the long term, increasing difficulty is expected in scaling both DRAMs and non-volatile memory (NVMs). The need for high density, fast, and new NVM structures is expected to increase, particularly to reduce power dissipation. Implementing such advanced, non-volatile structures will be a major challenge.

#### Strong Points

Very strong know-how of SOI technology, devices and its use implications in SRAM circuits, especially 1T-RAM.

#### Weak Points

Knowledge localized in excellence centers, need for dissemination.  
No industrial EEPROM in SOI up to now.

#### European Groups

Infineon, Germany

CEA-Leti and SOISIC, France (J.L. Pelloie): Contributor in PD and FD SRAM technology and design.

STMicroelectronics, France (P. Flatresse): Contributor in PD-SOI SRAM technology and design.

Polito, Italy (M. Casu): Contributor in PD-SOI design and methodologies.

EPFL/Innovative Silicon (P. Fazan): 1T-RAM patent and development

UCL, Belgium (D. Flandre): SRAM with ultra-low-static power dissipation

#### Conclusions and recommendations

SRAM circuits are fundamental for VLSI designs because of their large and always growing employment in SoC. It is fundamental to have at disposal memory generators (all views, from layout to HDL) and reliable models for design and simulation. This is a key point that the circuit design research community in the SOI field should pursue so as to facilitate the successful adoption of this technology by the EU industry.

As for microprocessors, the effort should be focused on embedded memory segment.

NVM (EEPROM) should be developed and offered on SOI to broaden application scope of mixed-signal products.

### 8.4.- Analog & RF

#### 8.4.1.- Analog & RF circuits and characterization techniques

#### Comments

A strong analog characterization basis exists in Europe. There is only one group dealing with analog characterization in US, but this group focused only on simulations and does not base their characterization on experimental results.

#### Strong Points

Unified methodology, which allows comparing different devices, has been developed. Advantages of non-doped and SOI double-gate MOSFETs devices for analog applications have been demonstrated.

#### Weak Points

Knowledge localized in excellence centers, need for dissemination.



### European Groups

UCL, IMEC, Southampton Univ., IMEP

### Conclusions and recommendations

Characterization technique, which allows to estimate analog performance starting from measurements performed on simple transistor structure, has been developed. The big advantage of this technique is that it allows to fairly compare very different devices (with different geometry, from different technology, etc.).

Wideband extractions allow to develop compact models, give insights about the physical phenomena and figure out the impact of some technological parameters on the device performance.

### 8.4.2.- HR Substrates & Crosstalk Analysis

#### Comments

High Resistivity Silicon (HR-Si) is foreseen as a promising substrate for radio frequency integrated circuits and mixed signal applications, but is known to suffer from surface effects and resistivity degradation near the insulating oxide. The use of SOI substrates provides better device isolation, reduced capacitance, reduced leakage, higher frequency operation and higher packing density.

The use of SOI with a HR-Si handle greatly minimises pad and interconnect parasitics of transistor transition frequency  $f_T$ . Thermal noise sets the lower limit of detectable signal in a receiver front-end. In this case, substrate noise enters via the pads or large area inductors and is amplified by the transistors. It has been shown that substrate induced thermal noise is minimised for Fully Depleted SOI (FDSOI) transistors on high resistivity handles, while on low resistivity substrates the noise is similar to that for bulk devices. It has been experimentally verified a reduced noise figure for transistors on HR-Si substrates.

#### Strong Points

The use of SOI substrate has the ability to reduce crosstalk.

SOITEC has achieved industrial demonstration of HR substrates with effective resistivity of 200 Ohm·cm at best.

UCL and QUB have lab-demo of HR substrates effective resistivity of more than 1000 Ohm·cm

UCL has a complete CMOS process fabrication line which allows fair comparisons between various Silicon and SOI substrates. It is flexible and allows fast prototyping.

#### Weak Points

New substrates developed by QUB and UCL not yet transferred to industry.

### European Groups

SOITEC, France

Queen's University, United Kingdom

UCL Belgium

### Conclusions and recommendations

Characterization methodology for the extraction of the substrate effective resistivity is available for fair comparison purposes. Extremely high resistivity substrates have been built and fully characterized. This new type of SOI substrates with passivated HR-Si handles offers considerable promise for RF analog applications.



SOITEC work has resulted in commercial large-diameter HR substrates with effective resistivity of 200 Ohm·cm. Therefore, from the material side, SOITEC is waiting for device guys a signal to invest for mass production.

In a near future, higher resistivity substrate (> 1000 Ohm·cm) demonstrated in EU labs on small diameter wafers and with only passive microwave test structures should be transferred to large-diameter CMOS platforms.

#### **8.4.3.- RF modeling (small signal, noise)**

##### **Comments**

The circuit modeling of RF will have to be extended to the 100 GHz range: Either extreme RF applications (77 GHz car radar, 60 GHz WLAN) or 30–40 GHz applications where (third harmonic) distortion is important. Models for active devices, including their parasitic elements, are crucial for good RF circuit modeling. However, the correct description of passive circuit components will need significantly more attention. Modeling of inductors, transmission lines and varicaps will include skin effects and other resistance increase at higher frequencies. The models for these (frequency dependent) effects should not contain any frequency-dependent components. This allows time-domain simulations in addition to frequency-domain simulations. For several larger (active or passive) elements the non-quasi-static effects will be significant and should be modelled accurately.

##### **Strong Points**

Models validated down to  $L=0.13\mu\text{m}$  and frequencies up to 30 GHz.

##### **Weak Points**

Proprietary models, not available in CAD tools.

Most of the modeling work has been done only for single-gate FD MOSFET.

##### **European Groups**

IEMN group (led by F. Danneville)

URV group (led by Prof. B. Iñíguez) FD SOI MOSFET

UCL group (led by Prof. D. Flandre)

##### **Conclusions and recommendations**

There are not many European groups working on the compact modeling of SOI MOSFETs in RF. The URV/UCL macro-model for RF FD SOI devices was successfully tested for frequencies up to 40 GHz and channel lengths down to  $0.13\mu\text{m}$ , but is only available in an internal version of ELDO. IEMN, through collaboration with those groups, have developed a model for RF noise in FD SOI MOSFETs, but is not available in any simulator yet. More efforts should be dedicated to PD SOI MOSFET modeling in RF. It would also be very wise to extend to RF the multiple-gate SOI MOSFETs models recently developed by several European groups.

The trouble of RF modeling is the integration in tools. RF modelling suffers the same problem as other MOS models, i.e. interest of groups such as Philips to extend their models to SOI, make them openly available and work with SOI experts.

#### **8.4.4.- Analog design**

##### **Comments**

SOI technology offers interesting advantages concerning analogue circuits. More particularly four domains of application for analogue circuits can be identified: 1) resistance to radiation, 2) high temperature 3) high-speed 4) low-voltage operation.



### **Strong Points**

Knowledge on analogue design present in the active groups.

### **Weak Points**

Not availability of commercial CMOS SOI processes in Europe yet.

### **European Groups**

UCL, EPFL and LETI.

### **Conclusions and recommendations**

The successful realizations of mixed-mode systems in Japan illustrate the potential of SOI. In Europe, the availability of state-of-the-art CMOS SOI processes will be the key for further development. Although analogue circuit design is a tough and challenging task, it will never drive the markets. So, processes targeting mixed-mode applications, allowing the integration of digital circuitry and embedded memories will make the decision. Analogue design will follow.

Therefore, Europe should focus their efforts in mixed mode applications. However, the bottlenecks of technology access, models, parameters and libraries should be solved first. Tools are not supported adequately. And when they are too late.

### **8.4.5.- RF design**

#### **Comments**

SOI is a very promising technology for RF applications. The intrinsic SOI isolation and the possibility to combine advanced SOI processes with high-resistivity substrates ( $\rho > 1000 \text{ ohms.cm}$ ) allow great improvements in terms of low-power consumption, passive devices and SoC integration.

#### **Strong Points**

Good background in the SOI RF characterization & modeling

#### **Weak Points**

Few RF SOI circuits already demonstrated

#### **European Groups**

UCL-CISSOID: RF characterization & modeling, Passive devices optimization, HR substrates, RF building blocks designs.

IMEP-LETI-ST: RF characterization & modeling, RF Switches, RF building blocks.

IEMN: Noise Measurements & Modeling.

#### **Conclusions and recommendations**

A good technology background exists in Europe concerning the characterization and the modeling of SOI RF devices. However, few circuits have already been demonstrated except by IBM in USA.

It is quite clear that Europe must focus their efforts on the RF design in SOI technology with emphasis on telecom applications and also on automotive.



## **CHAPTER IX. End-users & Industrial Applications.**

### **9.1.- Radiation-hard Products (Aeronautics & Space Applications)**

#### **Comments**

This could greatly affect the European Aeronautic and Space industry in case of commercial conflict with USA. US ITAR (restricted exportations rules for military reasons) regulations are putting an arbitrary economical pressure on European Space programs. EU is weak in nuclear science electronics fabrication.

#### **Strong Points**

High scientific knowledge exists in Universities and Research centers  
Applications exist (ESA, Alcatel-Aleniaspace, EADS...)

#### **Weak Points**

No industrial rad-hard-qualified technology in Europe based on SOI. All CERN chips for present experiments were designed on a IBM technology.

#### **European Groups**

Industrial European position in this field is very weak. Not any European semiconductor company is offering SOI-based processes or products.

#### **Conclusions and recommendations**

The EC, in coordination with ESA, could support existing European SOI foundries (X-Fab, STMicroelectronics, Atmel) to make their processes compatible with radiation-hard requirements. A first point could be to characterize the existing SOI processes and circuits designed on these processes under radiations. A second point would be to guaranty the durability of existing SOI processes in Europe (X-Fab, ST).

We feel a very strong demand of the aeronautic and space industries in Europe to have access to radiation-hard SOI process and products. If not done, this could dramatically affect European aeronautic and space independence with respect to US.

### **9.2.- High-temperature Products (Oil & Gas, Aeronautics & Space, Automotive)**

#### **Comments**

SOI for high-temperature is a hot strategic topic but there is not large European administrations investing in like DoD or DoE in USA.

#### **Strong Points**

Technologies & expertise are available.

#### **Weak Points**

The industrialization is still weak

#### **European Groups**

Four companies are offering SOI processes or products for high-temperature applications: X-Fab, Atmel, CISSOID, First Sensor Tech.

#### **Conclusions and recommendations**

High-temperature Electronics based on SOI could become strategic for the European industry (Oil & Gas, Aeronautic & Space but also Automotive). SOI high-temperature



electronics bases exist in Europe but the industrialization is still weak and should be improved through R&D projects or supporting companies active in this field.

The same kind of conclusions as for radiations-hard productions is arising for high-temperature applications. High-temperature SOI processes and products being sensitive technologies, they can be subject to US ITAR (restricted exportations rules for military reasons) regulations. These means that European industries (Oil & Gas, Aeronautic & Space or Automotive) using these technologies can be subject to export limitations. This is why it is very important to have these technologies available inside Europe.

### **9.3.- High-speed Products (Microprocessors and Data Communications)**

#### **Comments**

Microprocessors applications are pushing the most advanced SOI developments: new microprocessors architectures, advanced technology nodes, new SOI substrates (very thin film and 300mm wafers). Even if the substrates are developed and manufactured in Europe by Soitec and if a part of the microprocessors are manufactured in Europe by Freescale (in Crolles) and AMD (Dresden), the Microprocessor industry is led by US and Japanese companies. It is probably too late for European semiconductor companies to address these markets but they can take advantage of the last existing SOI developments in their applications and markets: Wireless, Automotive and telecommunications.

However, European start-up companies are emerging and offering digital design kits (Soisic) and very dense embedded memories (Innovative Silicon). These IP's can address general purpose or dedicated (display) microprocessors applications.

#### **Strong Points**

SOI microprocessors manufacturing facilities and design centers are located in Europe. Start-up companies in IP design are emerging.

#### **Weak Points**

No European microprocessor vendor.

#### **European Groups**

No companies developing SOI high-speed products. However, AMD microprocessors are manufactured in Dresden (Germany) and Freescale 90nm microprocessors will be made in Crolles (France). IBM has a SOI microprocessor design group in Bobelingen (Germany). SOISIC (France) is offering SOI digital design kits and Innovative Silicon (Switzerland) is proposing very dense embedded memories.

#### **Conclusions and recommendations**

SOI microprocessors applications are dominated by US Companies, having some activities in Europe. This is probably not the field were Europe has to compete. However, Europe has not to leave advanced SOI technologies to US, Japanese or Asiatic companies because SOI will bring huge benefits for low-power and RF applications where European companies are key players (Wireless, Automotive and Telecommunications).



#### **9.4.- High-voltage Products (Audio, Power Management, Automotive)**

##### **Comments**

Europe has a technology leadership thanks to Philips. Other companies are arriving with new technologies based on SOI, both for medium (smart power) and high power applications: Infineon, Atmel, X-Fab, Cambridge Semiconductor.

##### **Strong Points**

Good expertise and industrialization in Europe.

##### **Weak Points**

Industrial processes are not always open to fables companies

**European Groups:** Philips Semiconductor, Infineon, Atmel, X-Fab, Cambridge Semiconductor

##### **Conclusions and recommendations**

SOI, mainly for its isolation properties, is appreciated for high-voltage applications. SOI is used to make smart power chips (automotive, Audio, ...), high-voltage drivers but also high power devices (Lateral IGBT of Cambridge Semiconductor on a SOI Membrane).

This is very important for the automotive and power semiconductor applications, both markets where Europe has a strong position.

#### **9.5.- Ultra Low-voltage & Low-power Products (Watch applications)**

##### **Comments**

The scientific and design know-how exists in Europe but there is a lack of SOI processes available and a lack of industrialization.

##### **Strong Points**

Good scientific and design know-how.

##### **Weak Points**

Lack of industrialization.

##### **European Groups**

UCL, CISSOID and LETI on ultra-low-power circuit design.  
EM-Marin worked on technology developments.

##### **Conclusions and recommendations**

The great interest of SOI for ultra-low-power and ultra-low-voltage applications has been demonstrated in Europe and in Japan. Europe has a good scientific and design know-how but there is a lack of low-power SOI processes available and a lack of industrialization in Europe. A low-power SOI process available through a Multi-Project-Wafer (MPW) available in Europe should be of great interest.

Many applications of interest for EU industry would benefit from such developments in new fields such as wireless sensor networks, implanted bio-electronics, human health monitoring and diagnosis...

#### **9.6.- Microwave & RF Products (Wireless applications)**

##### **Comments**

The great interest of SOI for low-power and RF applications has been demonstrated in Europe in the frame of Research projects, in particular the T206 Medea+ project on



“SOI for low-power digital and RF” led by ST Microelectronics. In this project, process steps, devices, models and circuits were developed in 0.13 $\mu$ m Partially Depleted SOI. The great interest of high-resistivity SOI for RF applications was demonstrated by UCL (Cross-talk), LETI, CISSOID (Inductors, Varactors and 5GHz VCO) and ST (RF Switches). A MPW access to process would be made available to European research and industry.

**Strong Points**

Very Good scientific and industrial know-how in process development, devices optimization, modeling, and design

**Weak Points**

Lack of industrialization: ST Microelectronics 0.13 $\mu$ m PD SOI process is not yet industrially available.

**European Groups**

UCL, LETI, CISSOID, ST Microelectronics

**Conclusions and recommendations**

An advanced SOI process for low-power and RF applications could offer breakthroughs for the European wireless industry.

Open existing processes for MPW access and industrialization could produce new ideas and applications to emerge.

Capitalizing on the results and experience already obtained in MEDEA+ T206 project to address and develop more advanced processes, following both the “more More” (next technology nodes) and “more than More” (adding process options on existing processes) strategies.