THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

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HIGHLIGHT FEATURE

The Time is Right for SOI Technology Adoption

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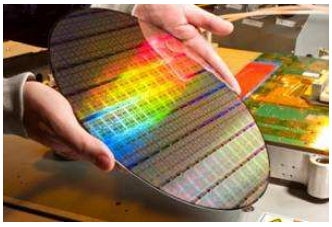
The time for Silicon-on-Insulator (SOI) technology has finally arrived. As process technology shrinks, the power density of chips is climbing. Alternate technology approaches are going to be needed to address this challenge. Mike Muller, , ARM CTO, at the March 25 EE Times "Designing with ARM" virtual conference postulated: given the same power budget used for the 45 nm design today, if an 11 nm design has 16X the transistors running at 0.6X the power, "I can actually use only 10 percent of them in my new design," Muller said. "The rest is dark silicon. We need to find ways of lighting that silicon up."

Fortunately, as Muller postulated, SOI technology is an obvious contender to meet the power density test. For seven process generations, SOI has been quietly serving high-performance applications such as enterprise servers, networking and storage systems, and game consoles delivering on challenging speed requirements consuming up to 40% less power than bulk silicon technology. With scores of SOI based products deployed in the marketplace, SOI is a time-tested technology with proven custom and digital design flows. In addition, a growing base of IP is becoming available for a new set of consumer product applications such as digital TV, high-performance mobile internet devices, printers, and ultralow-power applications such as wristwatches and automotive applications. In addition, SOI's favorable radiation-tolerant characteristics have been recognized by companies such as Boeing for extraterrestrial semiconductor applications.

So, what makes SOI process deliver this superior performance/power profile? Bulk technologies start with a single-crystal silicon substrate, the SOI starting material has an embedded oxide layer just below the silicon surface. The significance is a reduction in leakage current and power/performance advantages over devices designed and built in bulk wafers.



Internal studies at IBM have compared 45 nm SOI-based circuits to the same circuits in 45 nm bulk silicon showing yield 30% performance benefit using transistors of comparable leakage. For designs not requiring higher performance, the SOI advantage can be turned into a lower-power design point. Additional IBM studies indicate lower soft error rates are intrinsic to SOI technology, with a 5–7× improvement over bulk. Furthermore, SOI-based devices generally have better temperature sensitivity so that they can be operated at high temperatures and latch up does not exist because device isolation prevents parasitic bipolar device formation between FETs.

Last week the SOI Industry Consortium announced the launch of its "Ready for SOI Technology" program, a global initiative to broaden access to energy-efficient silicon-on-insulator (SOI) technology for the electronics industry. Recognizing that SOI technology has not reached its full potential in the marketplace, a core group of SOI Industry Consortium (SOIC) members: ARM, Cadence and IBM came together to address some of the perceived obstacles to wider adoption of SOI process technology. In 2008, GSA and SOIC conducted a survey identifying EDA tools, IP and education as barriers to adoption of this promising technology. Today, these issues are being addressed via the SOIC's aggressive program aimed building a broad and complete ecosystem for SOI design. At launch of the program, ChipEstimate.com fielded a web portal dedicated exclusively to SOI IP and boasting more than fifty IP elements from IBM, ARM, Cadence, Boeing and Synopsys. The rich set of IP available from IBM, has been silicon proven within its ASIC technology offering and is now available to foundry customers as well. In addition, designers can take advantage of IBM's SOI foundry offering with embedded DRAM. IBM's SOI technology with eDRAM is a key enabler for multi-core processors and other integrated circuits and can result in improved systems performance and energy savings for a range of applications including networking, printer, storage, consumer and mobile products. Today the ChipEstimate.com/soi portal can enable designers to evaluate SOI process technology against other technologies for their next design.

[*Source: Chipestimate.com*]

NEWS

IBM, ARM and Cadence act to make SOI chips cost-effective

IBM is working with ARM and Cadence to remove one of the biggest barriers to more widespread adoption of silicon-on-insulator (SOI) semiconductor process technology. SOI is known to have definite power and performance advantages over commonly used bulk CMOS process technology. But its mainstream adoption has been slow because of higher cost and a lack of process proven silicon intellectual property (IP).

Collaboration between IBM, ARM and Cadence, as part of the wider SOI Industry Consortium, will make semiconductor IP blocks proven on the IBM SOI process, such as memory, IO and power management, available for licensing. ARM has provided 18 IP blocks including memory compilers, IO libraries and power management functions. IBM's embedded DRAM IP is also included. The intention that the 50 IP block available at launch of the programme will be added two by further IP blocks from across the industry. Boeing and Synopsys are the next companies to provide IP to the programme.

According to Horacio Mendez, executive director of the SOI Industry, the aim of the IP library is to remove one of three barriers to what he called "mainstream adoption of SOI in the consumer and mobile phone markets". Another obstacle has been access to SOI process technology, but according to Mendez, this has been addressed with foundries such as IBM, Globalfoundries and Chartered offering services. The other main obstacle to adoption is the higher cost of the SOI process compared to equivalent bulk CMOS processes. "As we are seeing the complexity of bulk CMOS process increasing to match performance and power budgets we are seeing the cost of SOI falling," said Mendez.

According to a spokeswoman from IBM Microelectronics, there are already SOI devices in consumer products such as games consoles. "That gives us a data point about how the price differential is changing," said. "It is possible that there could be price parity between SOI and bulk CMOS within a few generations," said Mendez. But this is not likely to be the current 45nm generation where Mendez predicted the cost differential will be in "single digits". ARM offered its first physical IP libraries for IBM 45nm SOI process more than a year ago. These included standard cell, memory and I/O libraries for IBM's fully enabled 45nm SOI foundry. This IP is now commercially available.

[*Source: ElectronicsWeekly*]

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NEWS

Education to reduce barriers to SOI adoption

The SOI Industry Consortium has launched the 'Ready for SOI Technology' program to stimulate adoption of energy-efficient silicon-on-insulator (SOI) technology. A cornerstone of the program is education.

Initiated by IBM, ARM and Cadence, the 'Ready for SOI Technology' program aims to provide chip and system designers access to SOI design intellectual property (IP) and make this IP available through a SOI portal hosted on the ChipEstimate.com website.

And, to enable the formation of a complete ecosystem that enables designers to take full advantage of the benefits of SOI technology, IBM, ARM and Cadence decided to deliver educational tools such as trainings and seminars.

A survey conducted by the Global Semiconductor Alliance (GSA) and the SOI Consortium in 2008 highlighted the need for more SOI education and awareness. A question indeed asked what the biggest reason was for not evaluation or using SOI today, and the top reason cited was the perceived additional cost of SOI, followed by lack of design knowledge and then risk and IP availability.

This survey proved that education is key to reducing barriers to adoption, confirmed the need for a group dedicated to SOI to provide the knowledge and expertise needed to inform the industry and debunk present misconceptions.

"Making sure that we educate people is precisely what we are trying to do," stated Horacio Mendez, executive director of the SOI Industry Consortium. "Education is a broad perspective. We are trying to educate designers on how to design with SOI but also on how they can access the IP and the advantages of SOI."

[*Source: EETimes*]

[…] "We are trying to educate designers on how to design with SOI but also on how they can access the IP and the advantages of SOI." said Méndez.

NEWS

ARM CTO warns of dark silicon

ARM Moore's Law keeps marching relentlessly forward, thanks to engineers conjuring up increasingly clever tricks to push back against the laws of physics. According to ARM, in the last seven years mobile phones have shown a 50X improvement in talk-time per gram of battery, while at the same time taking on new computational tasks that only recently appeared on desktop computers, such as 3D graphics, audio/video, internet access, and gaming. Now you can use your Blackberry to watch streaming video from YouTube or play interactive online games while pretending to check your email.

Still, there's trouble in paradise. This Thursday, ARM's CTO Mike Muller will deliver the keynote address at EE Times' Designing with ARM virtual conference. According to Mike, despite process scaling down to 11 nm, fixed power budgets may soon make it impossible to utilize all the available transistors on a chip. Without fresh innovations, designers could find themselves at some point in an era of "dark silicon," able to build dense devices they cannot afford to power.

Muller makes his argument with the following numbers: Compared to a 45-nm die, 22 nm will enable a 4X die shrink; 11 nm, 16X. Again taking 45 nm as the reference point, the peak frequency at 22 nm can increase 1.6X and at 11 nm, 2.4X. All well and good. However, while power consumption may remain constant at 22 nm vs. 45 nm, at 11 nm it drops to 0.6. All this means that at a 45-nm power budget, at 22 nm only 25% of the silicon is exploitable and only 10% is usable at 11 nm. Clearly this isn't an acceptable trend line.

In his keynote Mike will detail both tactics and strategies for lighting up what would otherwise be "dark silicon." Silicon on insulator (SoI) will play a big role—the first ARM-based 22-nm test SoI chips taped out last October; SoI goes a long way toward addressing the leakage problem at smaller geometries. Energy-efficient and robust high-density memories will facilitate reduced operating and retention voltages. 3D silicon integration (3D ICs) will enable high levels of energy efficiency and performance improvements.

Other recommendations and predictions: Muller sees Neon++ as the future of vector processing, improving single-threaded performance and extending Neon's reach to new application domains. Stream programming on the GPU—using the OpenCL programming model—makes possible high-throughput computations on floating-point intensive applications. Mike sees MP++ as "the future of multi-core scalability" and in his talk goes into some of the architectural implications and scalable coherence techniques. He will also discuss the evolution of the SoC interconnect and some of the ins and outs of sub- and near-threshold circuit design.

On the strategy side Muller explains a new approach to dynamic voltage scaling, referred to as Razor, which is based on dynamic detection and correction of speed path failures in digital designs. The key idea of Razor is to tune the supply voltage by monitoring the error rate during operation. Muller proposes a combination of circuit and architectural techniques for low-cost, in-situ error detection and correction of delay failures. [*Source: Embedded.com*]

ANNOUNCEMENT

Extended deadline for ESSDERC-ESSCIRC 2010

The final extended deadline for ESSDERC and ESSCRIC 2010 is April 18th.

These conferences will take place in Sevilla (SPAIN) from September 13th to September 17th, 2010

The two conferences have been running together for several years and they provide an excellent annual forum for the presentation and discussion of most recent advances in solid-state devices and circuits both from industry and from academia. In 2010, the two conferences will have a common schedule and will share Plenary Keynotes Presentations, Joint Sessions, Tutorials on September 13th and Workshops on September 17th. Besides taking benefit from a thoroughly selected Technical Program and having a place to networking and interacting with peers from worldwide, conference attendees will have the opportunity of enjoying the not-to-miss city of Sevilla. With more than 3000 years of splendorous history, Sevilla is a modern european city with very well-kept, outstanding historical remaining from the Roman Empire, the Muslim Kingdoms and the Spanish Empire, nice climate and friendly, hospitable people.

REMEMBER:

Submission deadline for ESSDERC and ESSCIRC 2010 is April 18th

EUROSOI ANNOUNCEMENT

Looking ahead: EUROSOI2011

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada, Andalucía (Spain). It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

As a first step the Workshop website is now available at

http://granada2011.eurosoi.org

FEATURE

Are you ready for Silicon-on-Insulator technology?

By Clive Maxfield

Silicon-on-Insulator (SOI) refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing to reduce parasitic device capacitance and thereby improve performance.

SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide or (less commonly) sapphire. The choice of insulator depends largely on intended application, with sapphire being used for radiation-sensitive applications and silicon dioxide preferred for improved performance and diminished short channel effects in microelectronics devices.

In order to bring us all up to speed, the SOI Industry Consortium is launching a "Ready for SOI Technology" program, a global initiative to broaden access to energy-efficient silicon-on-insulator (SOI) technology for the electronics industry. With this program an initial offering of SOI intellectual property has been provided by IBM, ARM, and Cadence Design Systems. More IP has been added by Boeing and Synopsys, with an invitation extended to other developers to add to the growing SOI IP ecosystem.

SOI process technology can provide up to 30 percent chip performance improvement and 40 percent power reduction compared to bulk silicon technology. SOI is widely used today in market leading products found in data centers, offices, vehicles, homes and elsewhere in applications for computing, storage and networking, as well as for graphics-intensive game consoles. The Ready for SOI program is now making necessary design building blocks available to a broader population of chip designers seeking to harness SOI technology's benefits for new applications, including mobile and consumer products.

A key enabler for this effort is the new SOI Portal hosted on the popular ChipEstimate.com site at www.ChipEstimate.com/SOI. The SOI Portal provides chip designers access to available design building blocks and to the companies supporting chip development on SOI processes.

"ChipEstimate.com has become a critical resource to over 26,000 registered SoC designers by providing central access to over 200 of the world's largest IP suppliers and foundries," said Adam Traidman, General Manager at Cadence. "Our new SOI micro-site will serve as an invaluable resource to designers wishing to explore the benefits of SOI technology for their chip design projects."

To help IP and chip designers transition to SOI, the Ready for SOI program is sponsoring SOI Jump Start Training. This special training event will be hosted by Cadence on April 28, 2010 at the Cadence Engineering Center Auditorium, in San Jose, CA. Jump Start Training will also be available as both a live and recorded webcast.

[*Source: TechBites*]

"ChipEstimate.com has become a critical resource to over 26,000 registered SoC designers by providing central access to over 200 of the world's largest IP suppliers and foundries," said Adam Traidman.

NEWS

Soitec supplying SOI substrates to CSMC for display and other applications

Soitec The Soitec Group,the world's leading supplier of engineered substrates for the microelectronics industry, announced that the company has entered into an agreement to supply silicon-on-insulator (SOI) substrates to CSMC Technologies Corporation ("CSMC"), a leading pure-play specialty analog foundry based in China. Soitec is sampling SOI substrates for High Voltage (HV) and CMOS applications initially aimed at color plasma display panel (PDP) driver integrated circuits (ICs) and other mixed signal and analog applications. The company is seeing high levels of interest and support in China for SOI projects. SOI is a cost-optimized technology increasing device performance and reliability, while lowering power consumption. These advantages are an excellent complement to consumer electronics markets, as well as continued expansion into worldwide markets for automotive, RF/wireless, high-voltage, power management, photonics, imaging, lighting and more.

"With this agreement, CSMC will use Soitec's wafers on several major SOI projects for High Voltage and CMOS technology. We believe the partnership with Soitec will help us to provide a more cost-effective solution to our customers," said Filian Wu, VP of Analog Process Technology Development Center."

As the world's leader in SOI substrates, we are very pleased to collaborate with CSMC and will support their plans to ramp up SOI based products," said Paul Boudre, Chief Operating Officer (COO) of the Soitec Group. "Over the last two years, we have experienced a strong acceleration of interest in SOI substrates in China mainly by the majority of the largest local foundries and institutes. Today these development projects are moving to first production ramp up and we expect a significant growth of SOI based products in China in the coming years." [*Source: Soitec*]

"With this agreement, [...] we believe the partnership with Soitec will help us to provide a more cost-effective solution to our customers," said Filian Wu

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- Korean International Summer School on Nanoelectronics
Daegu, Korea.
April 7th - 10th, 2010

- 217 ECS Meeting
Vancouver, Canada.
April 25th - 30th, 2010

- 6th International SemOI Conference and 1st Ukrainian-French Seminar
Kyiv, Ukraine.
April 26th - 30th, 2010

- International Symposium on Circuits and Systems. ISCAS 2010
Paris, France.
May 30th - 2nd, 2010

- ESSDERC ESSCRIC 2010
Sevilla, Spain.
September 13th - 17th, 2010

- 218 ECS Meeting
Las Vegas, USA.
October 10th - 15th, 2010

- EUROSOI 2011 Workshop
Granada, Spain.
January, 2011