THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

EUROSOI Newsletter

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HIGHLIGHT FEATURE MEMS on SOI — Growing Fast and Faster

Adele HARS
Advanced Substrate News

In the latest ASN posting by Dr. Eric Mounier of Yole Developpement, "SOI for MEMS: A Promising Material", he notes that SOI MEMS is growing at a CAGR (2011-2015) of 15.6%, compared to 8.1% for bulk silicon-based solutions.

MEMS designers are doing amazing things on SOI – which would explain that impressive growth rate.

One of my favorites is Debiotech's tiny insulin NanopumpTM targeting diabetes, fabbed by ST. As Debiotech's Laurent-Dominique Piveteau noted, "…the use of SOI wafers for fabricating the Nanopump MEMS device has significant medical and economic advantages. The SOI-based structure allows for the highest reliability in the smallest possible package, enabling very tight control and precision of the pumping mechanism. The flow rate is steady, and it is insensitive to pressure, temperature, viscosity and aging. It also offers extreme dosing precision."

Reasons cited by other contributors for using SOI for MEMS include:

- Eliminating the stress problems common in polysilicon;
- Ensuring well-defined film thickness for more accurate oscillation frequency of moving parts;

VTI's SOI-MEMS multi-axis accelerometer is the "stride sensor chip" in the miCoach real-time training system (Courtesy: VTI Technologies, adidas and Samsung

- Providing greater surface and sidewall smoothness;
- Enabling thinner structures;
- Increasing thermal conductivity of MEMS components.

But the bottom line is that it's the most cost-effective solution for their state-of-the-art MEMS devices.

MEMS also figure in two of the most recent ASN Buzz postings:

Intels's new transistors have tiny pillars, or fins that rise above the chips's surface

- Freescale and Leti just celebrated 10 years of SOI-MEMS collaboration, which includes producing a million SOI-based accelerometers a year for airbag and ESC apps in the automotive market.
- SiTime has expanded its line of SOI-MEMS-based silicon timing solutions with the industry's lowest power high-frequency oscillator. With 85% market share and over 35 million devices shipped, SiTime says it is driving the $5 Billion timing market's transition to 100% silicon-based timing.

If you'd like to see more of the why's and wherefore's of SOI-MEMS apps, just type "MEMS" into ASN's search engine. You'll get dozens of pieces from and about leaders like ST, ADI, Denso, VTI, Tronics, IBM and more.

[Adele Hars is Editor-in-Chief at Advanced Substrate News and Director at High Tech International]

CONFERENCE FD SOI Workshop in Taiwan

The SOI Industry Consortium, CEA-Leti and Soitec organized the 5th edition of the FDSOI Workshop at the Ambassador Hotel, in Hsinchu, Taiwan on April 28 following the VLSI-TSA and VLSI-DAT conferences (April 25-27, 2011).

This workshop was co-organized by Dr. H. Mendez from the SOI Industry Consortium, Dr. O. Faynot from CEA-Leti and Dr. C. Mazure and Mrs. B.-Y. Nguyen from Soitec.

More information:

Http://www.soiconsortium.org

FEATURE

Photonics on the Move

George CELLER
Rutgers University

SOI is at the heart of silicon photonics. Here's an overview of past, present and future trends.

"probably nobody anticipated that SOI would be a perfect medium for short distance transmission and modulation of light beams", says Celler

The existence of Silicon Photonics owes much to serendipity. During the early years of the development of SOI wafer technology probably nobody anticipated that SOI would be a perfect medium for short distance transmission and modulation of light beams. Only in 1986 Richard Soref pointed out that SOI structure had the right properties for light confinement in near infrared1, and some years later Si waveguides started being designed.

A very large refractive index contrast between the Si and the SiO2 means that the light is very well confined inside the Si waveguide core, which can have sharp bends. This leads to very compact photonic integrated circuits (PICs) with densely spaced micron-scale photonic devices.

Silicon Photonics emerges

By coupling optical fibers with Si waveguides etched in SOI substrates, the light that is going into or coming out of such fibers can be processed.

In recent years the photonics community has developed all the devices needed for such processing, from light modulators and wavelength filters built in SOI to photodetectors made in germanium that was selectively grown on Si, all capable of handling data streams with a bandwidth of at least 10 Gb/s and often much higher.

Even the light sources, one missing component in the SOI device chain, are coming closer to Si.

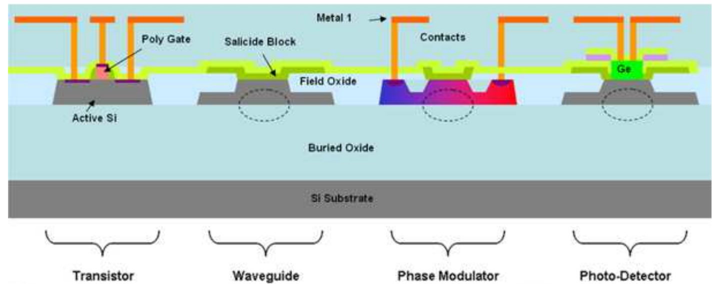
Just as multiple wavelengths can propagate in a fiber (wavelength division multiplexing or WDM), they can also propagate together in a Si waveguide, and devices to multiplex and demultiplex these data streams can also be built in SOI.

Power reduction is the key

We can expect that the future silicon PICs will be built with higher complexity and reduced cost, and with reduced power/bit of data. Fully integrated silicon photonics technology for transceivers used in short (10 – 100 m) and medium (1 km) range optical interconnects in data centers and supercomputers exists now at a few companies.

The enormous bandwidth requirements and power dissipation constraints in large IT systems will advance Si photonics for inter-board and inter-chip communication, and eventually for intra-chip links.

[Source: *Advanced Substrate News*]



CONFERENCE

2011 SOI Conference. Deadline for submission

Submission period for 2011 International SOI Conference is **May 16th, 2011**.

For over 35 years the IEEE International SOI Conference has been the premier meeting of engineers and scientists dedicated to current trends in Silicon-on-Insulator technology. Sponsored by the IEEE Electron Devices Society,the conference traditionally provides a forum for open discussion in all areas of SOI technologies and applications as well as the introduction of new developments presented in original papers presented at the technical sessions.

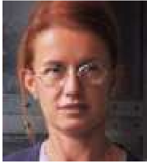
More information as well as a detailed programme can be found at the conference site:

http://www.soiconference.org

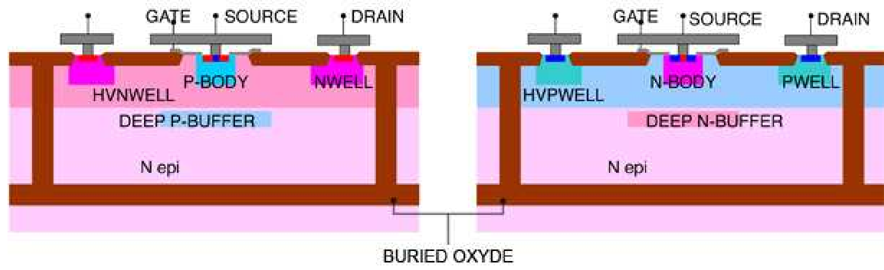
Tempe Mission Palms Hotel and Conference Center

FEATURE

Smart power saves power



Paola GALBIATI
STMicroelectronics



Cross Section of N-channel (left) and P-channel (right) power MOS

ST's newest SOI-based smart power technology delivers big reductions in power consumption in medical equipment, hybrid-electric-vehicle chargers and more.

There is an urgent need for semiconductor technologies that can drastically reduce electrical energy consumption in consumer and industrial appliances. At STMicroelectronics, we have developed new SOI-based smart power technology that will make a significant difference in the power consumption of a wide range of electronic systems – from new medical equipment to battery chargers in hybrid electric vehicles.

This new work began under the aegis of an advanced European R&D* project called Smart Power Management (PM). The SmartPM project aims to put a halt to the increasing demand for energy by means of intelligent consumption, which may even reduce power usage by up to 20 percent by the year 2020.

STMicroelectronics and 17 other companies developed a range of energy-saving electronic technologies. To qualify for the program, the technologies had to be both inexpensive enough for wide market penetration and dramatic enough to make a significant impact on overall electric power consumption.

ST has been solving critical power management challenges with SOI-BCD (Bipolar-CMOS-DMOS) processes for almost a decade now. The technology we developed under the SmartPM project is a next-generation variation of our world-leading BCD smart power technology, combining SOI with 0.16-micron lithography.

This new technology enables chip designers to combine high-density logic circuitry (1.8V and 3.3V CMOS) with full dielectric isolation and a component portfolio. Included are power MOSFET transistors that can operate up to 300V, low noise devices and high-value resistors, leading to ASICs that cannot be implemented using conventional bulk-silicon substrates.

Ultrasound Proof

In cooperation with General Electric and Sintef, ST has verified the feasibility of this new semiconductor technology by producing a demonstrator chip for ultrasound scanners** that can handle hundreds of channels with extremely low power dissipation.

The goal is to address the next generation of scanners, which will require thousands of channels for real-time, 3D imaging. In terms of power consumption and dissipation, this requires a leap far beyond the best technology available today.

Ultrasound probes are basically made of a transmitter, a receiver and an acoustic element to convert electrical signals to mechanical waves and vice-versa.

The state of the art in this market is measured by the number of transmitting/receiving channels integrated into a probe. On today's leading edge, a typical number of channels is 128 or 192 for a 2D image probe, but even thousands for 3D image and endoscopic segments. The driving circuitry is realized with discrete components, with a total power consumption of about 3W. And since the probes touch the patient, the temperature must remain below 40 °C.

The market, however, is pushing to significantly increase the number of channels to a target beyond 2800 channels with no more than 1.8W of total power consumption. This reduces the power dissipation per channel from 3W / 128 = 23.4 mW to 1.8W / 2800 = 0.64 mW: i.e. 40 times less.

Such a target is impossible with discrete components: hence a new technology was needed, which would permit the integration of 200V or more driving circuitry in a single chip.

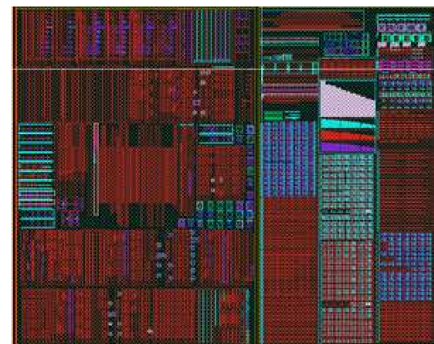
First silicon available

ST's new 0.18µm SOI-BCD technology with full dielectric isolation enables such integration. As such, it also enables many additional applications like power conversion, other electro-medical equipment, drivers for new batteries generation in electric cars and so on.

MOS devices for ultrasound machines need to handle different high-voltage classes: up to 300V, as well as 110V and 220V. Simulations helped to identify the best 220V components, and to ensure we could use the same masks for all classes.

Process integration and test chip layout have been completed. First silicon is now available, opening the door to the design of significantly more powerful yet dramatically more power-efficient end-user equipment.

Note: a related paper entitled "A Novel 0.16um – 300V SOIBCD for Ultrasound Medical Applications" will be presented at the 23rd International Symposium on Power Semiconductor Devices & ICs, to be held in San Diego May 23-26, 2011.



Top view of the test chip layout

[*Source: Advanced Substrate News*]

EURОSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- FD SOI Workshop
Hsinchu (Taiwan)
April 28th, 2011

- 219 ECS Meeting
Montreal (Canada)
May 1st-6th, 2011

- International Symposium on Circuits and Systems. ISCAS 2011
Rio de Janeiro, Brazil
May 15th-18th, 2011

- ESSDERC ESSCRIC 2011
Helsinki, Finland
September 12th-16th, 2011

- 2011 IEEE International SOI Conference
Tempe, Arizona (USA)
October 3rd-6th, 2011

- 220 ECS Meeting
Boston, MA (USA)
October 9th-14th, 2011

- 221 ECS Meeting
Seattle, Washington (USA)
May 6th-11th, 2012