

THEMATIC NETWORK
ON SILICON ON
INSULATOR
TECHNOLOGY, DEVICES
AND CIRCUITS.



EUROSIOI

Newsletter

VOLUME XV

AUG-SEPT, 2009

IN THIS NUMBER:

IBM's Power7 1
heats up server
competition at
Hot Chips

6th Internation- 1
al SemOI
Conference

High-end ser- 2
ver chips breaking records

Smaller, cheaper 2
cell phones possible

NXP Dual 3
Channel Class-D Amplifiers

Chartered to 3
start 32nm pilot runs in 4Q09

MOSIS Marks 3
Expanded Semiconductor Foundry Offerings

Cadence Validates 4
ARM Optimized Libraries for 45nm SOI Process

GlobalFoundries 4
outlines roadmap

Calendar 5

HIGHLIGHT NEWS

IBM's Power7 heats up server competition at

Hot Chips

 IBM Corp. walked away from Hot Chips conference with bragging rights to having the most muscular microprocessor with its Power7. The eight-core, 45nm chip is expected to set new watermarks in parallelism and cache that could translate into leading-edge performance for servers using it. Addressing the broader market for x86-based systems, Advanced Micro Devices will describe its 12-core Magny-Cours, its first to use a multichip module. Intel Corp. will detail its Nehalem EX, a souped-up version of the Xeon 5500 that debuted earlier this year.

Sun Microsystems, still waiting for approval of its merger with Oracle Corp., will present the latest version of its Sparc-based Niagara processor at the annual processor confab hosted by Stanford University.

When the dust settles, IBM likely will stand above the competition. The Power7 is expected to support as much or more cache, threads and memory bandwidth as any of the competition.

"I am sure Power7 will be the fastest processor around, probably faster than Intel's Nehalem in some benchmarks," said Nathan Brookwood, principal of market watcher Insight64 (Saratoga, Calif.).

Among its several advances, Power7 uses a mix of SRAM and IBM's embedded DRAM technology to pack on to the same die as the processor as much or more cache as any of its competitors. That's a big shift from

the past three Power generations that used cache on separate die in a multichip module.

The shift from the two-core Power6 to the 4-, 6- and 8-core Power7 drove the need for more memory, a change that took years of effort both in IBM's silicon-on-insulator process technology and in memory architecture, said Bill Starke, an IBM Power architect who has worked on four generations of Power chips.

"We knew when we hit this level of multicore design, we would have to make the shift," Starke said. "We've been talking about this for several processor generations," he said.

The eDRAM cache of more than 32 Mbytes, improved off-chip signaling techniques "and a few more ingredients," helped IBM get beyond the 300 Gbyte/second memory bandwidth of the Power6. In

addition, Power7 is said to pack as many as eight DDR3 memory channels.

"IBM will have far greater memory bandwidth than anyone else, and that matters because with multicore design the issues is getting data in fast enough to feed the beast and the Power7 beast will be well fed," said Brookwood. Early reports suggested Power7 had at least 16 Mbytes eDRAM. But the paper revealed IBM packed a whopping 32 Mbytes eDRAM as L3 cache on the 567 mm-square chip.

The Power7 is expected to scale back on the blistering 5 GHz data rate of the Power6 but ratchet up the support of multithreading from two to as many as four threads per core, the watermark previously held only by Sun's Niagara processors.

[Source: EETimes]

ANNOUNCEMENT

6th International SemOI

Conference and 1st Ukrainian-French Seminar



First announcement and call for papers for the 6th International SemOI Conference and 1st Ukrainian-French Seminar to be held from 26th-30th April 2010 in Kyiv (Ukraine) have just been launched.

The goal of the Conference is to

debate about the recent developments in nanometer down scaled Semiconductor-on-Insulator (SemOI) Systems which are basis blocks for modern high-sensitive sensors in a wide range of applications such as telecommunications, radiation control, biomedical instrumentation, Chemicals analysis, etc.

FEATURE

High-end server chips breaking records



Peter Glaskowsky

How would you like a single-chip microprocessor with more than four times the performance (on some applications) of Intel's best Core i7?

Then consider that up to 32 of these chips can be directly connected to form a single server, achieving four times the built-in scalability of Intel's next-generation Nehalem-EX processor.

That's IBM's widely anticipated Power7, which it described at last week's Hot Chips conference. But if you're interested, you'd better be prepared to spend a lot more than four times as much per chip. IBM isn't talking about pricing, but large Power servers can cost more than \$10,000 per processor.

What makes the Power7 so powerful? Each chip has eight cores,

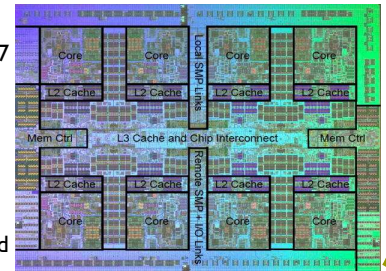
and each core supports four-way multithreading. There's 32MB of level-3 cache on the chip, made using embedded DRAM (eDRAM) cells. Most CPUs use SRAM for cache because it's generally easier to combine with high-performance logic, but DRAMs--with only one transistor per bit--offer compelling density advantages. IBM spent years developing a new kind of eDRAM that would work with SOI (silicon on insulator) manufacturing processes, and the Power7 is the most advanced product to use the new technology.

Interestingly, the Power7 cores run much more slowly than those in the Power6 processor, which I wrote about here in 2007 ("Live from Hot Chips 19: Session 1, IBM's Power6"). The Power6 was designed to run very fast using a long CPU pipeline in order to deliver the highest possible performance on each thread

of execution.

Maybe that strategy didn't work out as well as IBM hoped, because the Power7 returns to a more traditional microarchitecture with a shorter pipeline and much lower clock rates--though IBM didn't say exactly what those rates would be.

IBM did, however, promise that the Power7 would be roughly four times as fast as the Power6, chip for chip. Since it has four times as many cores, each of the new slower-clocked cores must still deliver about as much performance as those in the previous generation.



IBM spent years developing a new kind of eDRAM that would work with SOI (silicon on insulator) manufacturing processes, and the Power7 is the most advanced product to use the new technology.

NEWS

Smaller, cheaper cell phones possible

Ph.D. candidate Sataporn Pornpromlikit played a critical role in research at UC San Diego that made a big impact at a recent conference, and might provide manufacturers with the means for making cell phones both smaller and cheaper.

Pornpromlikit, who goes by the name Aui (pronounced way), was the lead author on the prize-winning paper, which was based on research carried out in the Power Amplifier Lab at UC San Diego's California Institute for Telecommunications and Information Technology (Calit2). The paper outlines a new method for integrating a cell phone's power am-

plifier on the same chip with the rest of its internal parts using standard CMOS technology.

CMOS, or Complementary Metal Oxide Semiconductor, is a low-cost integrated circuit process technology that has been driving the communications industry for the last few decades. Although the majority of cell phone circuitry has been successfully integrated onto a single silicon chip using CMOS, until recently the power amplifier -- the part of the device that amplifies the telephone signal -- needed a separate chip because of its high voltage requirement.

"Power amplifiers are among

the most power-consuming components in the transceiver and need to be designed for the best power efficiency to maximize the cell phone's battery life," explains Aui. "They also need the best signal quality and to provide the required large output power.

"With the low breakdown voltage limit allowed by the advanced CMOS process," he adds, "the power efficiency suffers severely."

But his design solves the problem, Aui says, by distributing the required voltage equally among stacked transistors to allow for safe operation, even with the highest power output.

[Source: *Physorg.com*]

The paper outlines a new method for integrating a cell phone's power amplifier on the same chip with the rest of its internal parts using standard CMOS technology.

NEWS

NXP Dual Channel Class-D Amplifiers Bring Power

Efficient Concert Hall-Like Sound Into the Vehicle



NXP, the independent semiconductor company founded by Philips, extended its leadership in vehicle audio entertainment, introducing a new family of dual channel Class-D amplifiers that deliver cutting-edge sound quality and energy efficiency. The new NXP TDF8599 Class-D amplifier family operates with maximum output power from 70 – 130 watts (250 watts mono), significantly reducing power dissipation in the vehicle head-unit when compared to traditional Class-AB amplifiers and ensuring more efficient heat management. With an extremely high dynamic audio range, the new Class-D amplifiers transform the vehicle entertainment experience, delivering concert hall-like sound

quality for best-possible audio enjoyment on the move. The TDF8599 amplifier family complements NXP's existing broad portfolio of highly energy-efficient Class-D amplifiers, and were developed to fit our customers' highest requirements.

Christian Seidel, Group Leader Hardware, Mechanics & Layout Audio System Engineering Group from Harman Becker Automotive Systems in Straubing, Germany said, "The TDF8599 series gives us the opportunity to dramatically reduce the power dissipation in our multichannel audio amplifiers and at the same time increase the sound quality to satisfy our customers' needs."

[Source: Business Wire]

NEWS IN BRIEF

Chartered to start 32nm pilot runs in 4Q09, sources say

Chartered Semiconductor Manufacturing is scheduled to launch its 32nm process technology in the fourth quarter of 2009, and move to 28nm in the first half of 2010, industry sources have revealed. The Singapore-based foundry is expected to update its process advancement at an upcoming technology forum in Taiwan.

Chartered's 28nm node will be based on high-k metal-gate (HKMG) technology from the IBM-led joint-development alliance, and built on a gate-first approach.

[Source: Digitimes]

NEWS

MOSIS MARKS EXPANDED SEMICONDUCTOR FOUNDRY OFFERINGS WITH

SHUTTLE RUNS FOR SILICON-ON-INSULATOR (SOI)



The MOSIS Service, a leading provider of semiconductor fabrication solutions, announced that it has expanded its relationship with IBM to now include silicon-on-insulator (SOI) technology at multiple advanced lithography nodes. MOSIS is offering IBM's 45-nm SOI technology on 300mm wafers and IBM's 180-nm SOI technology on 200mm wafers. MOSIS customers now have a low-cost route to prototyping and low-volume production with leading-edge SOI foundry technologies that provide enhanced performance and very high integration capabilities.

The initial 45-nm shuttle run is scheduled for September 1, 2009. IBM's 45-nm 1250 technology is the company's sixth generation of leading-edge SOI technologies and the first 300mm SOI technology to be offered through the MOSIS Service. This process provides significant transistor performance improvement (up to 30 percent) over traditional bulk technology at the same lithography node. The 45-nm SOI process offers four tran-

sistor options (Regular, High Vt, Super High Vt, Ultra High Vt), in addition to up to 11 metallization layers. A range of SRAM (Static Random Access Memory) and embedded DRAM (Dynamic Random Access Memory) options are also available, as well as a number of ESD (Electrostatic Discharge) protection options and high-quality passive elements. In addition to providing excellent isolation for analog circuit performance, this SOI offering can reduce the circuit area by up to 25 percent relative to bulk CMOS, which cuts the cost of overall semiconductor content.

The first available 180-nm SOI shuttle run has successfully been completed, with the next shuttle run scheduled for September 14, 2009. The low insertion loss and high isolation makes this technology an ideal choice for components such as RF switches that perform the function of On/Off devices in wireless applications like cell phones, WiMAX and WLANs (Wireless Local Area Networks).

"MOSIS is delighted to partner with IBM

to now offer SOI foundry technologies," said Wes Hansford, Deputy Director of MOSIS. "The 180-nm 7RF SOI technology provides a very compelling alternative to GaAs (Gallium Arsenide) technology for RF switches, while the 45-nm SOI technology delivers outstanding performance while maximizing power efficiency and minimizing overall chip size for SOC (System-on-Chip) applications. By broadening our portfolio, MOSIS provides a single interface between designers and a greater range of foundry services, thereby enabling our clients with a faster and lower-cost route to market."

"This is a natural next step for our partnership with MOSIS and makes our advanced SOI technology accessible to an even broader array of innovators," said Regina Darmoni, IBM's Director of Analog/Mixed Signal & Digital Foundry. "MOSIS provides IBM with additional channels to market, and we are looking forward to this further expansion of our fabrication solutions to enable a new generation of advanced devices and clients."

[Source: MOSIS]

NEWS

Cadence Validates ARM Optimized Libraries for 45nm SOI Process

“These new silicon-validated libraries 45nm SOI libraries enable the creation of power efficient SOC’s, while reducing development time and cost.” says Tom Lantzsch.



Cadence Design Systems, Inc., the leader in global electronic design innovation, announced that they have validated a new generation of ASIC libraries from ARM using the Cadence® Encounter® Digital Implementation System targeting IBM’s 45-nanometer silicon-on-insulator (SOI) manufacturing process. The development marks another milestone in a multiyear collaboration enabling efficient utilization of IBM’s low-power, high-performance SOI technology for next-generation designs.

“Our collaboration with Cadence on the early validation of their tools will ensure design readiness for customers of IBM’s 45nm SOI technology. Collectively, ARM, Cadence and IBM offer a

reliable design platform wherever speed, functionality and low power consumption are needed,” said Tom Lantzsch, vice president, physical IP division, ARM. “These new silicon-validated libraries 45nm SOI libraries enable the creation of power efficient SOC’s, while reducing development time and cost.”

The ARM 45nm SOI libraries were developed using the Cadence Virtuoso® custom design platform 6.1 and validated on multiple designs in the Cadence Encounter Digital Implementation System, a complete RTL-to-GDSII design environment that features the Si2 Common Power Format (CPF) for low power design, native signoff-in-the-loop for interconnect extraction, timing, power, and signal integrity

plus fully integrated Cadence design-for-manufacturing (DFM) technology. The entire Cadence end-to-end design, implementation, and verification solution is proven to fully support the SOI manufacturing process.

“The collaboration among Cadence, ARM and IBM is vital to designers targeting our SOI technology,” said Richard Busch, director, IBM ASIC Products. “It’s imperative that these libraries are designed, verified and implemented in close correlation to our SOI process so designers can achieve the full benefits of higher performance and lower power consumption versus bulk CMOS technologies.”

[Source: Cadence]

NEWS

GlobalFoundries outlines roadmap, plans to break fab ground



Taking on UMC, TSMC and others, foundry startup GlobalFoundries Inc. has outlined its process roadmap and disclosed plans to break ground on its new U.S. fab.

The foundry startup will break ground on the fab. As previously reported, it plans a \$4.5 billion, 300-mm fab in Malta in N.Y.’s Saratoga County that is expected to come online in 2012 with 35,000 wafer starts per month at full capacity.

GlobalFoundries (Sunnyvale, Calif.) is the silicon foundry venture created by the spinoff of Advanced Micro Devices Inc.’s manufacturing operations and backed by an investment from Advanced Technology Investment Co. (ATIC) of Abu Dhabi. It officially opened for business in

March.

In the meantime, the company is ramping up its existing fabs in Dresden, Germany, which were once part of AMD. As expected, the company is going after the leading-edge foundry business, thereby competing against UMC, TSMC, and, to some degree, its fab partners in Chartered and Samsung. GlobalFoundries is part of IBM Corp.’s “fab club,” which includes Chartered, IBM, Samsung and others.

“We feel we have an opportunity” despite the downturn, said Tom Sonderman, vice president of manufacturing systems and technology at GlobalFoundries. “Customers are looking for choices at the leading-edge.”

At present, the company has one fab, dubbed Module 1. It is processing 45-nm wafers, based on silicon-on-insulator (SOI) technology and immersion lithography. Its only custo-

mer is AMD.

For critical layers, GlobalFoundries’ main lithography vendor is ASML Holding NV. “We are also engaged with Nikon and Canon,” Sonderman said. For low-k at 45-nm, the company is using Applied Materials Inc.’s Black Diamond films

[Source: EETimes]

REMEMBER:

First announcement and call for papers for the 6th International SemOI Conference and 1st Ukrainian-French Seminar



EUROSIO Network

Thematic network on silicon on insulator technology, devices and circuits.

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

The **EUROSIO** network embraces a broad range of research areas related to **Silicon-On-Insulator** technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). **EUROSIO** aims at federating the existing research work on **SOI** topics and at providing an appropriate communication channel between academic groups and industrial production centres.

CALENDAR

- European School On Nanosciences & Nanotechnologies

Grenoble, France.

August 23rd - September 12th, 2009

- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference

Athens, Greece.

September 15th - 19th, 2009

- 2009 IEEE International SOI Conference

Foster City, USA.

October 5th - 8th, 2009

- 216th ECS Meeting

Vienna, Austria.

October 4th - 9th, 2009