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EDITORIAL



Sorin Cristoloveanu
IMEP, Grenoble (France)

About 8 years ago, I was asking myself a number of questions:

- How prominent will the SOI technology be in the future landscape of the microelectronics?
- How good are we Europeans in SOI?
- How many are we all together?
- Are we collaborators or just competitors?
- What is the quantitative rate and qualitative impact of the European papers at international conferences, and in particular at the IEEE SOI Conference?
- Is there any SOI bridge somewhere in Europe?
- Is there any serious competitor for SOITEC in the arena of SOI wafer fabrication?
- Why the European industry is so shy and does not go into the SOI chip business?
- Why then are LETI and IMEC developing such wonderful technologies?

Over a memorable diner in Granada, Paco Gamiz double checked my calculations. They looked accurate. We asked further verification by our good SOI friends: Olivier (Faynot), Denis (Flandre), Steve (Hall), Bruno (Ghyselen), Stefan (Bengtsson), Francis (Balestra), Jean-Pierre (Colinge... from US) and many others (a bottle of wine for everybody I

missed). Anyway, they all confirmed.

The conclusion was straightforward: we need to initiate a European SOI conference. Actually, 'resuscitate' rather than 'initiate'. A European SOI Workshop had been organized already, 2-3 times in Grenoble, in the 80's. It dried out because nobody wished to take the relay in a discipline which, at that time, looked more like a wonderful speculation.

We decided to call this event EuroSOI. Then, Paco said "This is good, as good as any good tapas can be. But just tapas is not enough, we need meat." A few seconds later, the idea of European SOI network emerged. Paco took care of the rest.

We wanted to design a network with whatever ingredients a network can carry. We got in contact with all European SOI groups and the returns rated between positive and enthusiastic. Then we asked benediction

from Brussels and you know by now the rest of the story. The EuroSOI network started officially a couple of years later.

EuroSOI workshops were organized yearly with reasonable audience, good papers and, even more importantly, a positive gradient in quality. Selected papers were published in extensive versions in Solid-State Electronics. Since the network performed and well, the European Union Commission gave us a 'plus' and accepted to help us to continue. This is how we became, early this year, EURO-SOI+.

We did lots of useful things, at technical and human interaction levels. More can be done and will come next. After reviewing the past and the future, I feel that SOI is like 'Return to Forever'. The problem is that these brilliant musicians do not have a clue about SOI. Why don't we invite them at EuroSOI?

ANNOUNCEMENT

Proposals of Scientific

Exchange Visits funded by EUROSIO+ approved

At the end of May, and in the hopes that this initiative—in addition to increasing the mobility possibilities of scientists—will result in an enhancement of collaborations and information exchange, EUROSIO+ launched fundings for scientific exchanges and research visits.

Once the evaluation process finished, and considering that

the applications received fulfilled the requirements, the Management Board of EUROSIO decided to approve all of them.

Further information and results can be found at the EUROSIO web site <http://www.eurosoi.org>.

NEWS

Soitec Ready With Ultrathin SOI Wafers

**Soitec**

Soitec (Bernin, France) announced at SEMICON West that it has qualified silicon on insulator (SOI) wafers with ultrathin buried oxide (BOX) and silicon layers. The SOI wafers — named XUT+ to describe the ultrathin top silicon and BOX layers — are aimed at both partially depleted (PD) and fully depleted (FD) devices, including multi-gate transistor architectures, such as finFET and trigate, that may play a role at 22 nm and beyond.

CEO André-Jacques Auberton-Hervé said, “The very thin oxide layer allows backside control [of the channel], which

is important for limiting the threshold voltage variability. That is a necessity for embedded SRAMs in particular because the threshold variability is being affected by the difficulty in controlling the number of dopants inside the channel. Even one atom can affect the threshold voltage,” he pointed out.

The ultrathin SOI layers may permit technologists to create planar structures with a back gate underneath the channel, providing many of the advantages of finFETs while pre-

serving the easier-to-manufacture planar structure, he said.

Also, the thin BOX is required for the SOI-based floating body cell (FBC) memories being developed by Toshiba Corp. (Tokyo), Intel Corp. (Santa Clara, Calif.) and others. At the recent 2008 Symposium on VLSI Technology in Honolulu, Intel researchers presented research on a FBC memory for embedded cache on microprocessors.

[Source: Semiconductor International]

“The ultrathin SOI layers may permit technologists to create planar structures with a back gate underneath the channel”, André-Jacques said.

NEWS

Nvidia Joins SOI Industry Consortium



Nvidia Corp., the world’s largest supplier of graphics processing units, has

joined the SOI Industry Consortium. Joining the organization may mean that the fabless developer of semiconductors is looking forward to design chips that will be made using silicon-on-insulator technology.

“Nvidia is pleased to join the SOI consortium. We are looking forward in participating on the advancement of such an innovative technology and its applications to future products,” said John Chen, vice president of technology and foundry operations at Nvidia.

Even though Nvidia is a fabless developer, hence, does not operate its own fabs, it is tremendously interested in rapid development of chip manufacturing technologies and design tools so that to be in position to continue creating leading-edge graphics processing units as well as other chips.

The SOI Industry Consortium, which was formed in October 2007 by a group of companies from across the electronics industry, is aimed at accelerating silicon-on-insulator innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption.

Nvidia brings the SOI Consor-

tium membership to twenty three companies. Other members include: AMD, Applied Materials, ARM, Cadence Design Systems, CEA-Léti, Chartered Semiconductor Manufacturing, Freescale Semiconductor, IBM, Innovative Silicon, KLA-Tencor, Lam Research, Magma Design, Samsung, Semico, Soitec, SEH Europe, STMicroelectronics, Synopsys, TSMC, Tyndall Institute, UCL and UMC.

The SOI Industry Consortium is open to any company, organization or academic institution with an interest in SOI.

[Source: X-bit labs]

Joining the organization may mean that Nvidia is looking forward to design chips that will be made using silicon-on-insulator technology.

EVENTS

European School On Nanosciences & Nanotechnologies

The fifth session of this European school, which will be held this year in Grenoble (France), will begin the fourth week of this month and will last until September 13th.

This 3 weeks course is aimed at providing training for graduate students, postdoctoral and junior scientists from European universities and laboratories in the field of NANOSCIENCES and NANOTECHNOLOGIES in Physics, Biology and Chemistry. The academic and practical courses cover the elaboration, functioning and characterization of nano-

objects. The program emphasizes the role of laboratory courses (half of the program is devoted to practical work).

The proposed programme is endowed with two key points. The first is interdisciplinarity, since research in Nanoscience demands a combination of various skills in physics, chemistry and biology. Learning the basic knowledge necessary to communicate with other scientific communities is a determining ingredient to create new nano-objects and to connect them to the macroscopic world.

The second point emphasises the role of laboratory courses. In general, summer schools do not address this issue which is, however, of fundamental importance both for basic science and for applications.

The program is structured to highlight the fundamental and technological advances in Nanoelectronics and at the interface between Physics and Biology.

The two sessions will run in parallel but they will share common lectures and practicals.

EUROSUI NEWS

First EUROSUI Working Group Meeting

One of the important goals of EUROSUI+ is to boost the exchanges of information about the Fully Depleted SOI Technology developed by LETI (which makes reference to devices that are fabricated on ultra-thin SOI films and coupled with high-K and metal gates).

In this framework, EUROSUI planned the organization of three Working Group Meetings, first of which will be held in Grenoble by October or November. The final date and the list of speakers will be conveniently announced through the next volume of this

Newsletter (September) and also through the EUROSUI website.

All EUROSUI+ beneficiaries will attend these meetings and in addition, different experts from the rest of EUROSUI partners and from Industrial Advisory Board members will also be invited.

The global idea is to organize a technical event with several presentations in order to see:

- What is available today with regard to LETI FDSOI technology?
- What would be needed to go further?

ANNOUNCEMENT

SOI Inventory list elaboration

EUROSUI is currently elaborating an inventory of SOI training material in order to create a database of books, publications, short courses... that could be useful to synthesize the present SOI knowledge.

You may forward to eurosui@ugr.es any material that you consider to be outstanding or just indispensable.

This call is open to all EUROSUI members as well as to other members from the International SOI Community.



EUROSUI NEWS

First Call of the EUROSUI 2009 Workshop

EUROSUI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007) and Cork 2008, EUROSUI 2009 will be held at Chalmers, Göteborg. It

will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

EUROSUI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

Information about the 2009 Workshop is now available at the Workshop web site

<http://chalmers2009.eurosui.org>

Abstract submission and registration will be available in October.

CHALMERS

MC2
Microtechnology and Nanoscience

It is becoming
urgent to involve
design people in
next future to
work using SOI
devices and SOI
technology

EUROSUI NEWS

Short course on Circuit Design

Last January and in the framework of the EUROSUI Workshop held in Cork, it was organized a first short course dedicated to Multi-Gate Silicon on Insulator Technology. The Short Course Lectures were given by world-leading experts and focus on the opportunities offered by Multi-Gate FETs and on the challenges they pose in the field of fabrication, device physics and circuit design.

And now a second short course is being prepared to be held during the EUROSUI 2009 Workshop in Göteborg. One of the main conclusions

of the Workshop held in Cork was that it is becoming urgent to involve design people in next future to work using SOI devices and SOI technology. As a consequence, this second Short Course in Chalmers will be devoted to Circuit Design on SOI substrates.

A final list of lecturers will be announced in September.

The importance and relevance of design is clearly a matter of consideration as can be seen for example in the last number of the *Advanced Substrate News* which devotes several articles to SOI Design written

by important figures such as Remy Pottier, Kevin Kranen, Tony Bonaccio or Michael White.



EUROSIO Network

Thematic network on silicon on insulator technology, devices and circuits.

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

The **EUROSIO** network embraces a broad range of research areas related to **Silicon-On-Insulator** technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). **EUROSIO** aims at federating the existing research work on **SOI** topics and at providing an appropriate communication channel between academic groups and industrial production centres.

CALENDAR

- **European School On Nanosciences & Nanotechnologies**

Grenoble, France.

August 24th - September 13th, 2008

- **Third SINANO Device Modeling Summer School**

Bertinoro, Italy.

September 1st - 5th, 2008

- **38th European Solid State Device Research Conference and 34th European Solid State Circuits Conference**

Edinburgh, United Kingdom.

September 15th - 19th, 2008

- **2008 IEEE International SOI Conference**

Hudson River Valley

New York, USA

October 6th - 9th, 2008

- **First EUROSIO Working Group Meeting**

Grenoble, France

October-November, 2008

- **EUROSIO 2009 Workshop**

Chalmers University of Technology

Göteborg, Sweden

January 19th - 21st, 2009

<http://chalmers2009.eurosoi.org>