



HIGHLIGHT NEWS

Fully depleted SOI shows its stuff in CPU design

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ARM

Cortex M0 paper design suggest that FDSOI could be a strong contender at 20 nm.

The The Silicon-on-Insulator (SOI) Industry Consortium this morning revealed results of an analysis showing a strong advantage for fully depleted SOI (FDSOI) over bulk silicon at 20 nm.

Researchers at ARM Ltd designed a Cortex M0 CPU core using FDSOI cells characterized by IBM at its Albany, NY, fab. The ARM team then analyzed the design for performance at various operating voltages. They found that at 0.9V, FDSOI offered about the same performance at 20 nm as a good bulk planar LPCMOS process. But at lower operating voltages, FDSOI showed significantly higher performance gains than bulk when compared to a previous-generation bulk process.

By 0.7V-still a viable operating voltage-the ARM team estimated designers would gain 25% in performance by moving from the previous node to 20-nm LPCMOS, but 80% by moving to 20-nm FDSOI. The comparison was based on the 30K gates of logic

in the M0 core, placed and routed using standard tools.

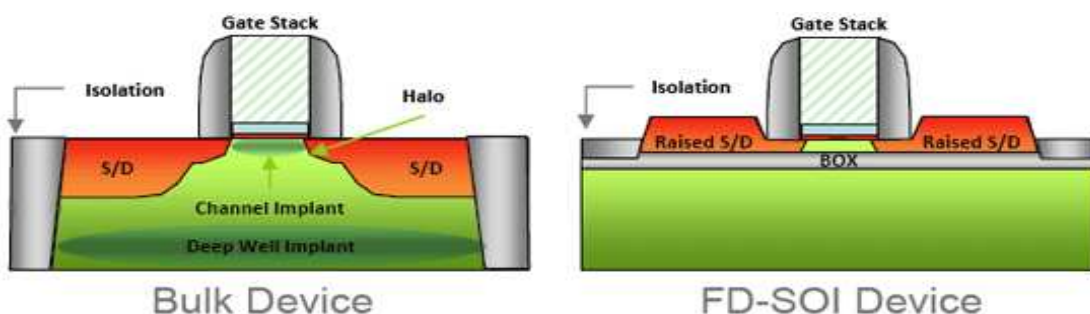
Consortium executive director Horatio Mendez said that FDSOI SRAM cells were stable at these low voltages, as well. "Our analysis of the memory cell indicates it is stable at voltages 150 mV below the minimum stable voltage for 20-nm bulk CMOS," he claimed. This could be a very significant point in the aggressive power-management strategies used in mobile devices. The immediate importance of the findings will be for developers of mobile devices, Mendez asserted. By giving designers access to operating voltages in the range of 0.7V at high performance, FDSOI could enable a substantial jump in both capability and battery life. Mendez explained that FDSOI FETs display a steeper sub-threshold characteristic than bulk silicon FETs: in effect, they switch faster. This difference becomes more pronounced as you compare the transistors at lower supply voltages. "In many cases," Mendez said, "you can lay out fewer fingers in the FDSOI cell and still meet your delay requirements." This compactness in turn brings further savings in metal resistance and

parasitic capacitance, all contributed to speed improvements and/or power savings.

The results are promising, but Mendez pointed out that they are first steps in a long journey. The FDSOI library ARM used was characterized with real wafer measurements at IBM. But ARM hasn't tried to fabricate the M0 design. There are still not market-ready libraries or RAM compilers for FDSOI, although work is reportedly under way. Nor is there a high-volume supply yet for the special FDSOI wafers, which must have an incredibly thin top silicon layer. Soitec is expected to make an announcement soon in this regard.

There is process work to do, as well. Current FDSOI FETs are simple transistors without strain engineering, and hence limited to relatively low speeds-in the low GHz region. Much opportunity remains for device engineering. And the process will generate new, probably simpler, design rules.

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The fully depleted SOI transistor at 20 nm is significantly simpler than even a simplified version of the bulk CMOS transistor.

FDSOI could enable a substantial jump in both capability and battery life

NEWS

Fully depleted SOI shows its stuff in CPU design (cont.)

This simplicity could be the technology's greatest strength. Because the gate in a FD transistor completely controls the entire channel region down to the insulating box layer, the channel does not require an implant in order to achieve acceptable performance. Without the implant, the fabrication process is significantly simpler-perhaps enough simpler to compensate for the added cost of the wafers with this one point-and the entire problem of Random Dopant Fluctuation,

with its huge impact on the variability of transistor threshold voltage, all but vanishes. Also, because the active channel extends all the way down to the box, there is virtually no charge trapping in the region under the channel, and hence the notorious SOI memory effect does not exist. This means that designers can work with normal CMOS timing files and timing tools without special provisions for the SOI process. Design teams can simply drop the FDSOI models into their existing flow.

The ARM announcement adds a significant new data point to the debate over the future of process technology at 20 nm and beyond. With FDSOI showing the potential for superior performance, simpler and more robust design, and no need for problematic structures such as finFETs, the weight of the argument for an FDSOI future appears to be growing.

[Source: EDN]

CONFERENCE

FD SOI Workshop in Taiwan

*New FD-SOI workshop
April 28, 2011 - Taiwan*

> [View the presentations](#)

The SOI Industry Consortium, CEA-Leti and Soitec organized the 5th edition of the FDSOI Workshop at the Ambassador Hotel, in Hsinchu, Taiwan on April 28 following the VLSI-TSA and VLSI-DAT conferences (April 25-27, 2011).

This workshop was co-

organized by Dr. H. Mendez from the SOI Industry Consortium, Dr. O. Faynot from CEA-Leti and Dr. C. Mazure and Mrs. B.-Y. Nguyen from Soitec.

More information: <http://www.soiconsortium.org>

REMEMBER:

2011 International SOI Conference deadline for contributions is May 16th

CONFERENCE

2011 SOI Conference. Deadline for submission



Submission period for 2011 International SOI Conference is **May 16th, 2011**.

For over 35 years the IEEE International SOI Conference has been the premier meeting of engineers and scientists dedicated to current trends in Silicon-on-Insulator technology. Sponsored by the IEEE Electron Devices Society, the conference traditiona-

lly provides a forum for open discussion in all areas of SOI technologies and applications as well as the introduction of new developments presented in original papers presented at the technical sessions.

More information as well as a detailed programme can be found at the conference site:

<http://www.soiconference.org>



Tempe Mission Palms Hotel and Conference Center

FEATURE

SOI: It's Elementary, My Dear Watson



Adele HARS

Advanced Substrate News

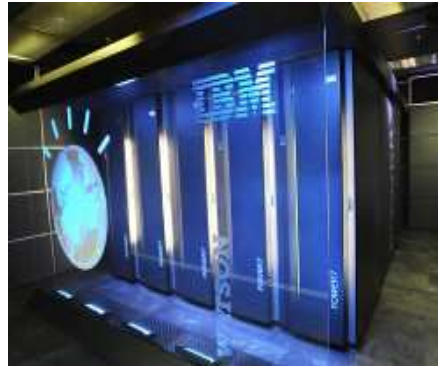
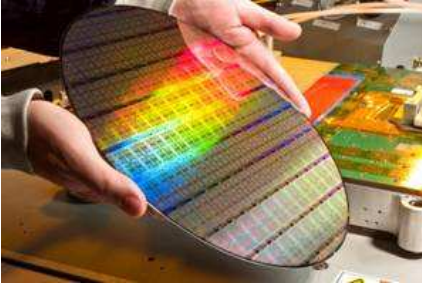
The other night, IBM's "Watson" super-computer beat the world's two best players in the popular "Jeopardy" game show, in which the contestants are told the answer, but then have to figure out the right question. In that spirit, here's an ASN spin on the game:

Category: semiconductor design & manufacturing.

Answer: The starting substrate for the Power7 processors in IBM's Jeopardy-winning "Watson" supercomputer.

Question: What is SOI?

Yes, Power7 is the 4th generation of Power processors that IBM has based on SOI. (The first was the Power4 – dual core, 174 million transistors/processor; 0.18µm copper + SOI – that IBM introduced 10 years ago.)



So why SOI? Well, first consider the size of the thing, and the performance and power involved. Then read on, because there's more to it than that.

Here are the Power7 specs:

- 45nm SOI
- 1.2B transistors
- 32MB onchip eDRAM shared L3
- 8 processor cores
- 12 execution units per core

For Watson, you have to keep multiplying. Watson is a cluster of 90 standard, commercially available IBM Power 750 servers – each with four Power7 processors. Each of those processors has eight 3.55-GHz cores, for a total of 2880 Power7 cores. The system has a combined total of 16 Terabytes of memory and can operate at over 80 Teraflops (trillions of operations per second).

OK, so SOI is helping with speed and power – that's clear.

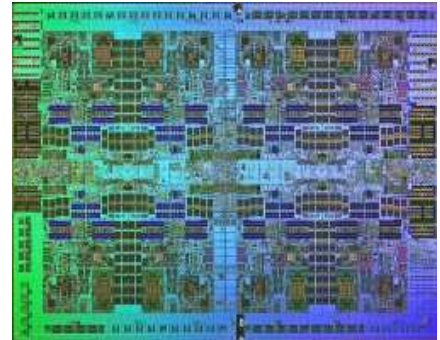
But in an ASN article five years ago (!), IBM Fellow Subramanian S. Iyer explained the importance of SOI in the memory part of the chip design equation. At that time, memory (mostly SRAM) was taking up almost 75% of the chip, so the push was on to shift at least some of that toward smaller, more stable and power-efficient embedded DRAMs (eDRAM).

As Dr. Iyer said, "The complexity added is about half in SOI compared to bulk for deep trench based eDRAMs. [...] We expect the use of eDRAM to proliferate to SOI in the 45nm generation."

Here is a cross section of IBM's 45nm SOI trench cell. The buried oxide is used to completely isolate the capacitor plate from the device.

What do you think of that?

[Source: Advanced Substrate News]



NEWS

Steve Longoria joins Soitec as SVP of Worldwide Strategic Business

Development to drive FD-SOI adoption



Soitec (Euronext Paris), the world's leading supplier of silicon-on-insulator (SOI) and advanced solutions for the electronics and energy industries, today announced the appointment of Steve Longoria to Senior Vice President Worldwide Strategic Business Development. An industry veteran with extensive experience and a pro-

ven track record primarily at IBM Microelectronics, Longoria joins Soitec's leadership team with responsibility for strategic business development activities worldwide, to drive FD-SOI adoption. This appointment comes at a very strategic time for the company, as the SOI Industry Consortium recently announced the substantial advantages of FD-SOI for next-generation

mobile and consumer applications.

"With his extensive knowledge of the overall microelectronics business and deep understanding of the role substrates play in chip design and manufacturing, Steve Longoria is a perfect fit for our senior management team," says Paul Boudre, Chief Operating Officer of Soitec.

[Source: SOITEC]



EUROSIO Network

Thematic network on silicon on insulator technology, devices and circuits.

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

The **EUROSIO** network embraces a broad range of research areas related to **Silicon-On-Insulator** technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). **EUROSIO** aims at federating the existing research work on **SOI** topics and at providing an appropriate communication channel between academic groups and industrial production centres.

CALENDAR

- ULIS 2011

Cork (Ireland)
March 14th-16th, 2011

- ESSDERC ESSCRIC 2011

Helsinki, Finland
September 12th-16th, 2011

- FD SOI Workshop

Hsinchu (Taiwan)
April 28th, 2011

- 2011 IEEE International SOI Conference

Tempe, Arizona (USA)
October 3rd-6th, 2011

- 219 ECS Meeting

Montreal (Canada)
May 1st-6th, 2011

- 220 ECS Meeting

Boston, MA (USA)
October 9th-14th, 2011

- International Symposium on Circuits and Systems. ISCAS 2011

Rio de Janeiro, Brazil
May 15th-18th, 2011

- 221 ECS Meeting

Seattle, Washington (USA)
May 6th-11th, 2012