

THEMATIC NETWORK
ON SILICON ON
INSULATOR
TECHNOLOGY,
DEVICES AND
CIRCUITS.



EUROSIOI

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EDITORIAL



Francisco Gámiz
Professor
Univ. Granada (Spain)

Happy New SOI year!!

With the arrival of the new year, EUROSIOI holds its annual meeting as every year. And it goes the seventh. The small "baby" who was born in Granada in January 2005, comes back again home, six year later, but with the same enthusiasm, and much closer to the achievement of our goals. This last year there was plenty of good news for SOI community.

There are many fields where SOI technology shows all its potential to circumvent the problems found in bulk technology: i) Shrinking the conventional MOS transistor below the 22nm-node, ii) the continuous demanding for low power consumption in ubiquitous mobile applications, iii) new memory designs, iv) high-temperature and power electronics, and so on. The steady work of the SOI community is demonstrating everyday that this technology can gain a higher portion of the electronic market. However, researchers have to face new challenges. The combination of hard work, imagination and creativity will lead us to success.

At this point, EUROSIOI initiative plays its main role: EUROSIOI network was born as the meeting point where all these efforts should converge. Since its beginning in Granada (2005) and touring through Grenoble (2006), Leuven (2007), Cork (2008), Chalmers (2009) and Grenoble (2010), the workshop served as the ideal forum for inspiring discussions and to foster strong interactions among specialists in different fields.

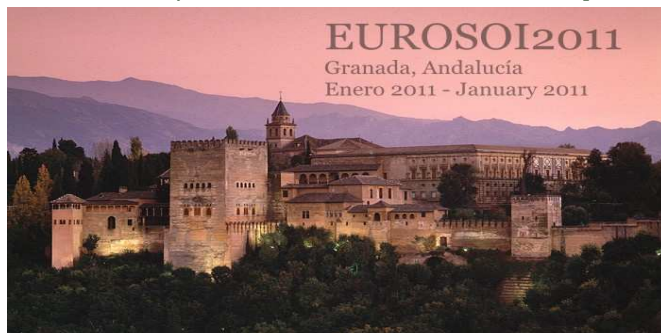
Following previous experiences, we have prepared an informal, lively

meeting with space for short presentations within a framework of larger discussion sessions. Relevant speakers have been invited to present the state-of-the-art in different fields of SOI. Dr. Carlos Mazure, from SOITEC, will open the conference describing the bright future of the FDSOI technology. Then Prof. Max Fischetti, from UTDallas, will take us as far as we can go. Prof. Carl Das, from IMEC, will introduce us in the Europractice network. Last, but not least, Mrs Gisele Roesems, from EU Commission, will talk about the future European research projects in the Nanoelectronics arena, formulating the strategy for the coming years. A Rump session chaired by Prof. Francis

Balestra, from IMEP, promises to be an exciting brainstorming.

Before the Workshop, and following the tradition, we have organized an interesting training course. The lectures are given by six experts covering the areas from technology, memories, imagers, low-power and photonics. It will take place on Monday, January 17th. We would like to highlight the magnificent venue where the Workshop will be held. We are sure that the "Parque de las Ciencias" will create a warm atmosphere prone to the exchange of scientific and technical ideas.

[Francisco Gámiz is Coordinator of the EUROSIOI+ Network]



CONFERENCE

EUROSIOI 2011:

great reception among participants



Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSIOI 2011 will be held at Granada this month **from January 17th to January 19th**.

It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample

room for informal discussions.

A large number of participants have been confirmed so far. All of them are welcome and invited to join us in what we expect to be a very pleasant conference.

Participation of students is especially encouraged through special prizes offered to them.

All the information at:

<http://granada2011.eurosoi.org>

NEWS

Material Effects: Trading Performance For Power

Ann Steffora Mutschler

Power impacts everything, even when it comes to semiconductor manufacturing materials. While bulk CMOS technology still reigns supreme, there are a number of advanced materials being suggested as replacements when it runs out of steam at around 15nm, including silicon on insulator (SOI)—particularly in combination with FinFET multigate structures on SOI—silicon germanium, gallium nitride, and aluminum nitride

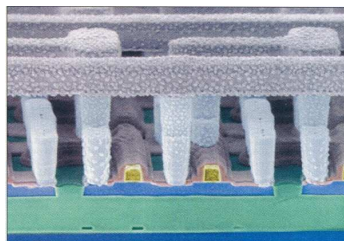
Most promising is SOI, already in use by IBM and AMD, which uses a layered silicon-insulator-silicon substrate instead of conventional silicon substrates to reduce parasitic effects and improve performance. Specifically, SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide, offering improved performance and diminished short channel effects in microelectronics devices. SOI can be implemented in two forms: partially depleted and fully depleted.

Jamil Kawa, group director of R&D in Synopsys' implementation group, emphasized that SOI is not new. "It has been with us for a long, long time. It has a lot of proven benefits, yet it never became mainstream.

He explained that SOI could be

compared to bulk CMOS by a rule of thumb: you can buy either a node in power for the same speed, or a node in performance for the same power. For example, comparing 90nm SOI to 90nm bulk, if they are running at the same clock frequency, the 90nm SOI will have the lower leakage characteristics of the 120nm bulk. Another way of looking at it is if the SOI is operating at 90nm with the same power budget that a bulk is allowed to consume, then it can give the performance that the next-generation (65nm bulk, in this example) will provide.

While it appears to be a simple formula that is carried from node to node to node, SOI didn't it catch fire as everybody thought it would mainly because of cost. "Given the lack of wide-scale adoption, the cost of initial wafers was more expensive and cost is extremely sensitive in our industry," he explained.



SOI Chip.

A second obstacle to SOI adoption has been the history effect inherent in the technology. There

is no substrate with SOI. It is oxide. Therefore, charge accumulates and has nowhere to go, and this alters the behavior of the device over time. Guardbanding is used to get around the history effect. "If you want to go conservative by guardbanding 15%, all the advantages in speed that you got by going SOI you've given up by going conservative. There are techniques to alleviate that, but bulk has remained the easy way out, a proven technology, cheaper, with a lot of momentum in terms of history of use," Kawa noted.

SOI is gaining renewed interest, however. At 20nm and 15nm, CMOS leakage is a big problem.

FinFETs are being looked at, sometimes in combination with SOI, as well. "At 15nm, you don't have too many choices. Bulk is more or less dead. If you insist on going with planar, you go the SOI way. Or you go the FinFET way. There is also a third variation, which will most likely gain hold, which is FinFET on SOI. Nothing is ruled in or out yet, but the excessive variability of bulk at extremely advanced nodes is giving a second life to SOI. The verdict is still out so I'm not advocating one course or the other, but the move toward FinFETs on bulk or FinFET on SOI is clearly the way to go in terms of leakage control," Kawa added.

[Source: Low-Power Engineering]

SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide, offering improved performance and diminished short channel effects in microelectronics devices.

CONFERENCE

General Information about EUROS01 2011



A set of tickets corresponding to conference lunches (only Tuesday and Wednesday) and Gala Dinner (Tuesday) will be provided to

each participant at the moment of registration.

Gala Dinner restaurant is at walking distance from the Parque de las Ciencias. After Gala Dinner a bus service will carry

participants to the Sacromonte for a Flamenco Show. At the end of it a shuttle service will be available to every official Hotel.

(Nazaries, Alhama and Luna)

PROGRAMME

Training Course Programme and Key-Note talks of EUROSOI 2011



As in previous editions of EUROSOI Workshop, this international event covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and applications oriented engineers.

Typical topics include:

- (1) Synthesis of advanced SOI wafers (Ge, SiGe and strained layers, SOI heterostructures)
- (2) Materials evaluation, properties of ultra-thin films and buried oxides, defects and stress, interface quality
- (3) SOI MOSFETs: characterization, modeling and simulation of typical mechanisms, parameter extraction, reliability issues
- (4) Circuit design, process and applications: low power/voltage and RF circuits, innovative memories, high voltage devices, imagers, sensors, photovoltaics and

MEMS

(5) More than Moore perspectives: multi-gates, 3D stacks of devices and circuits, nanowires, NEMS, tunneling transistors, heterogeneous integration etc.

For 2011 edition EUROSOI is trying its best and now putting the final touches.

The final programme for the Training Course, Key-Note Talks and Workshop has been scheduled and is now available:

Monday, January 17th. Training Course. Tutorial.

- 9.15h-9.30h: Introduction and Tutorial Overview. *F. Gámiz (University of Granada)*
- 9.30h-10.30h: SOI solutions for next technological nodes. *Prof. Sigfried Mantl, FZJülich, Germany*
- 10.30h-11.30h: ETSOI Technology. *Dr. Bruce Doris, IBM, USA*
- 12.00h-13.00h: CMOS-SOI-MEMS Imagers. *Prof. Y. Nemirovsky, Technion, Israel*
- 15.00h-16.00h: SOI Low-power applica-

tions. *Dr. N. Sugii, LEAP, Japan*

- 16.00h-17.00h: Memories on SOI. *Dr. Malgorzata Jurczak, IMEC Belgium*
- 17.30h-18.30h: SOI Photonics. *Dr. Jean Marc Fedeli, LETI, France*
- 20.00h-21.30h: Welcome Reception at Hotel Nazaries

Tuesday-Wednesday, January 18-19th. Workshop

Key-Note Talks.

- Readiness of FDSOI technology platform: overview. *Dr. Carlos Mazure, SOI-TEC, France*
- Issues on the Physics of Electronic Transport in 10 nm-scale SOIs: "How Far Can We Go?" *Prof. Max Fischetti, UTDallas, USA*
- EUROPRACTICE. *Prof. Carl Das, IMEC*
- Nanoelectronics: a bright future? *Mrs. Gisele Roesems-Kerremans, Deputy Head of Unit Information Society and Media / Nanoelectronics European Commission.*

CONFERENCE

Student Grants for EUROSOI 2011



SOI 2011 Workshop, **EUROSOI has given 15 grants to Ph.D. students** who have submitted a contribution to EUROSOI workshop.

To foster the participation of students to the Training Course and to EURO-

SOI has given 15 grants to Ph.D. students who have submitted a contribution to EUROSOI workshop.

The grant will consist on **the waiver of the registration fee (tutorial and Workshop) and the accommodation** (4 nights of hotel at Hotel Luna, Granada) from Sunday, January 16th to Thursday, January 20th, 2011.



EUROSOI 2011.

IMPORTANT DATES:

- Jan. 17th, 2011: Training Course.
- Jan. 18-19th, 2011: Workshop.

CONFERENCE

Free Entrance to the Parque de las Ciencias to badge Holders



The EUROSOI Workshop is held at the Parque de las Ciencias, which is an interactive museum of over 70.000 m² located a few short minutes from the historic city centre of Granada, with one of the most varied offers for cultural and scientific leisure in Europe.

El Parque de las Ciencias has several areas or different rooms starting from the con-

ception of the universe and the cosmos to the fascinating phenomenon of life that is contained in the Biosphere. There are many activities and attractions for children.

The Organizing Committee has reached an agreement thanks to which all participants can enjoy free entry during EUROSOI 2011 to visit it on presentation of their Conference Badges.



Detail of the Parque de las Ciencias in Granada



EUROSIO Network

Thematic network on silicon on insulator technology, devices and circuits.

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

The EUROSIO network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSIO aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

CALENDAR

- EUROSIO 2011 Workshop

Granada, Spain.

January, 17th-19th, 2011

- SEMICON Korea 2011

Seoul, South Korea.

January 26th - 28th, 2011

- CDE 2011

Palma de Mallorca, Spain

February 8th-11th, 2011

- ISS Europe 2011

Grenoble, France.

February 27th - 1st, 2011

- Ultimate Integration on Silicon Conference (ULIS)

Cork, Ireland

March 14th-16th, 2011

- 219 ECS Meeting

Montreal (Canada)

May 1st-6th, 2011

- International Symposium on Circuits and Systems. ISCAS 2011

Rio de Janeiro, Brazil.

May 15th - 18th, 2011

- ESSDERC ESSCRIC 2011

Helsinki, Finland.

September 12th - 16th, 2011

- 2011 IEEE International SOI Conference

Tempe, Arizona (USA)

October 3rd-6th, 2011

- 220 ECS Meeting

Boston, MA (USA)

October 9th-14th, 2011