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## HIGHLIGHT NEWS

## AMD's Opteron 4100s march into x64 price war



The big guns are already on the field in the x64 server processor war, and the troops are finally going all in with today's launch by Advanced Micro Devices of its entry "Lisbon" Opteron 4100s.

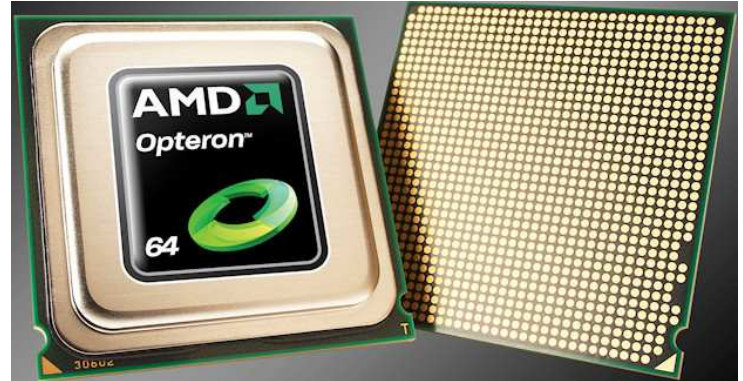
The Opteron 4100s are similar in many respects to the "Magny-Cours" Opteron 6100s that entered the battle against Intel's "Westmere-EP" Xeon 5600 and "Nehalem-EX" Xeon 7500 processors in March. Both chips are implemented in a 45 nanometer silicon on insulator process and manufactured by GlobalFoundries, the chip foundry that AMD spun out last year.

The Lisbon cores are quite similar to those used in the six-core "Istanbul" Opteron 2400 and 8400 processors from a year ago, with the transistor counts and processor areas being essentially the same, as are the cache memories. The big change is the shift from DDR2 to DDR3 memory for the integrated memory controllers. The Istanbul chips already supported HyperTransport 3 (HT3) point-to-point interconnect links, although the chipsets that the Istanbul talked to did not. (They had a backwards compatibility mode).

The Magny-Cours chips, which come in variants with eight or twelve cores per socket, basically cram two Lisbon processors side-by-side in a single chip package and slap them into a new G34 socket that is serviced by AMD's own chipsets. The Lisbon chip comes with either four or six cores per socket on a single die. Both AMD processors have 64 KB of L1 data and 64 KB of L1 instruction cache per core, plus 512 KB of L2 cache per core. The Lisbon chip has 6 MB

of L3 cache per processor package, and the Magny-Cours, being a double-stuffed socket, has 12 MB of L3 cache per socket.

The Opteron 6100s are aimed at



standard platforms that need lots of cores, clocks, and memory to support big databases or server virtualization hypervisors that in turn have lots of virtual machines running atop them. On these machines, raw performance and performance per watt are the two key metrics. Which is why AMD created the Opteron 6100s to support both two-socket and four-socket servers with the same chips and chipset.

Although, if you think about each physical chip as its own processor and look at the HyperTransport links coming into each socket, you could argue that what AMD has really done with the Opteron 6100s is crunch an eight-socket box into four sockets and a four-socket box into two-sockets.

This is a great strategy for customers who pay for their software based on socket count – and if you want to make a cheap four-socket box that can compete against Intel's more expensive Xeon 7500s. These latter chips from Intel have

Itanium prices and scalability, but Xeon instruction set compatibility, and AMD figured that by crunching down the socket count on Opteron processors by a factor of two

by doubling up the processors for the Opteron 6100s while at the same time creating an inexpensive, low-power server lineup for single- and dual-socket servers using the Opteron 4100s was the best way to undercut both the Xeon 5600s and the Xeon 7500s. The market will decide if this was indeed the right move.

What AMD has said this year, and what is no doubt true, is that it needs to get more market share in the server racket and it has to compete on price and performance to do that. However, it may just be that what many server customers want more than anything now is memory expandability within a 2P or 4P box, and the memory controllers inside the Opteron 4100 and Opteron 6100 processors can't address more than 512 GB, and a number of server OEMs, wanting to catch the server virtualization wave, have put two-socket and four-socket Xeon 7500 machines into the field that address 1 TB or more of memory.

[Source: The Register]

NEWS

## Silicon-on-sapphire transducers



Ellison Sensors has expanded its range of pressure transducers and transmitters. Using silicon-on-sapphire sensor technology and the latest digital electronics, the new range of process pressure transmitters and transducers is one of the most advanced in the market.

The range is aimed at industries requiring process pressure measurement including requirements such as high temperature or those requiring sensors with higher levels of resolution and

better long-term stability.

Silicon-on-sapphire technology is known for its superior accuracy and replaces solid state silicon and silicon-on-insulator technologies. The sapphire measuring diaphragm eliminates the insulation break down and the instability that is found in silicon pressure sensors, enabling the transmitter to operate at high temperatures. Sapphire is elastic with no measurable hysteresis, giving these transducers excellent repeatability.

The GS4200 USB digital pressure



transducer is powered from the USB port of a PC. Data is displayed on the PC and can be logged and recorded, making this an ideal solution for pressure measurement tests and requirements.

[Source: SA Instrumentation & Control]

Silicon-on-sapphire technology is known for its superior accuracy and replaces solid state silicon and silicon-on-insulator technologies.

NEWS

## EDA Consolidation Continues



The EDA Consortium recently announced a

second consecutive quarter of sequential revenue growth for overall electronic design automation (EDA) revenues. For Q4 2009, EDA industry revenues of \$1.26 billion grew 8.1% over the quarter while declining 4.2% over the year. The consortium noted that the biggest upticks came in the categories of CAE, IC Physical Design, and semiconductor intellectual property (IP).

No wonder, then, that Synopsys is continuing with its acquisition spree. The company recently acquired the intellectual property provider Virage Logic Corporation for nearly \$315 million. Synopsys believes that high-quality IP will remain key for "enabling designers to reduce integration risk and speed time-to-market." It is hopeful that the Virage acquisition will broaden its portfolio and help it to address the market in providing a quick way to incorporate

standard functions into their systems-on-chips (SOCs). Last fiscal year, Virage reported revenues of \$47.4 million. I agree with Daniel Nenni that the acquisition will give Synopsys a near monopoly in the design enablement space and

Synopsys is looking to strengthen its position in system-level design and verification and to enhance its field-programmable gate arrays (FPGA)-based prototyping solutions through this acquisition.

Meanwhile, the company announ-

The consortium noted that the biggest upticks came in the categories of CAE, IC Physical Design, and semiconductor intellectual property (IP).

Synopsys, Inc.



make it a bigger threat to competitors such as Cadence and Mentor, although not so much to ARM.

Synopsys also acquired high-level synthesis technology from Synfora, Inc. Synfora's technology enables designers to create and synthesize IC building blocks from a description written in the C or C++ programming languages.

ced mediocre Q2 results. Revenues for the quarter were relatively flat at \$338.1 million and EPS dipped to \$0.41 from \$0.45 a year ago.

Synopsys is also continuing to expand its existing product portfolio with products such as Yield Explorer (continues on next page)

NEWS

EDA Consolidation Continues (cont.)

which accelerates yield ramp by diagnosing yield issues during design for 90-nanometer and 40-nanometer design. Existing products are getting good reviews, and the company's Galaxy Design platform won the EDN Magazine Innovation Award.

The company projects revenues of \$330 million–\$338 million with EPS of \$0.36–\$0.38 for the current quarter. For the year, it projects revenues of \$1.340 billion–\$1.355 billion with EPS of \$1.52–\$1.62.

The stock is trading at \$20.87 with a market capitalization of \$3.09 billion. It touched a 52-week high of \$23.74 in November of last year.

Synopsys' competitor, Cadence, also recently made a rather expensive acquisition. Cadence acquired Denali, a privately held leading provider of EDA software and intellectual property provider for \$315 million. The transaction is expected to expand Cadence's solution portfolio to "deliver efficient and cost-effective system component modeling and IP integration."

Cadence Design Systems, Inc.



Sanjay Srivastava, Denali's CEO, I believe owned most, if not all of the company, so he had a nice payday.

Cadence's Q1 revenues of \$222 million were higher than the previous year's \$206 million. During the quarter, the company earned \$0.02 a share compared with \$0.10 a year ago.

It too is expanding its product portfolio and launched a comprehensive silicon-on-insulator (Sol) Design Hub, a new Web portal that will help lower barriers to adoption of Sol technology by reducing initial start-up costs, reducing time to mar-

ket for the Sol intellectual property, and improving design quality. I am hearing that some EDA players are trying to get into the SaaS model of delivering software, but don't know for sure if that initiative is coming from Cadence. It's possible.

The company projects revenues of \$215 million–\$225 million with a loss of \$0.03–\$0.05 a share in the current quarter. For the full year, it expects revenues of \$865 million–\$900 million with EPS of \$0.05–\$0.15.

The stock is trading at \$5.79 with a market capitalization of \$1.66 billion. In October of last year, it reached a 52-week high of \$8.18.

[Source: Sramana Mitra on Strategy]

NEWS

EUROSOI 2011, starting engines



Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada, Andalucía (Spain) from January 17th to January

19th.

It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

More information at <http://granada2011.eurosoi.org>

REMEMBER:

Early registration deadline for ESSDERC ESSCIRC 2010 is July 28th

ANNOUNCEMENT

Finalizing details for ESSDERC / ESSCIRC 2010 in Sevilla



The 40th European Solid-State Device Research Conference (ESSDERC) and the 36th European Solid-State Circuits Conference (ESSCIRC) will be held in Sevilla on 13 - 17 September 2010.

The aim of the ESSDERC and the ESSCIRC conferences is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits.

ESSDERC and its sister conference ESSCIRC are governed by a single Steering Committee. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts, and circuit and system designers. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC will share Plenary Keynote Presentations and Joint Sessions bridging both



Detail of the Cathedral in Sevilla.

communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions.

[...] “there are a few things you need to know about timing and signal-integrity analysis”, according to an August 25 webinar presentation by ARM and Cadence.

“SOI may provide new avenues to enable efficient design that provides optimal power management”, says the author

## FEATURE

## ARM, Cadence Webinar: How SOI Impacts Timing and Signal Integrity

By Richard Goering You probably know that silicon-on-insulator (SOI) technology offers lower power and/or better performance than bulk CMOS, and that qualified IP libraries are available. But what's the impact on the digital design flow? Fairly minimal, but there are a few things you need to know about timing and signal-integrity analysis, according to an August 25 webinar presentation by ARM and Cadence.

Entitled "Are You Ready for Silicon On

Insulator Design Process," the webinar was presented by Mike Jacobs, senior product manager at Cadence, and Remy Pottier, head of SOI marketing and business development at ARM. The webinar was the second in a series of Digital Implementation and Signoff webinars that will be rolling out over the next few weeks. I blogged separately about the first webinar, which covered on-chip variation and statistical timing analysis.

As Remy noted, ARM has IBM 45nm SOI physical IP libraries available today, and expects to roll out a 32nm library in the fourth quarter. He also pointed to the wide variety of third-party IP currently available at the Chipestimate.com SOI Portal. He believes that SOI is ideal for gaming, networking, and base station markets, and is increasingly attractive for mobile phone applications.

## FEATURE

## SOI the Holy Grail solution for addressing the power gap in advanced SoC designs?



By Remy Pottier

According to some industry pundits Silicon on Insulator (SOI) technology clearly enables more power efficient SoC designs. But is this advanced manufacturing technology the Holy Grail solution for addressing the power gap between performance and battery life in advanced SoC designs?

What are the factors behind the power gap? Well, let's start with the obvious – design complexity. You don't have to look very far to see that consumer and embedded devices are becoming more intelligent and supporting the latest in robust features. From the iPad to home entertainment, advanced functionality is abundant in products that just a few years ago were one step above dummy terminals. In parallel, products are finding themselves risking extinction fueled by hybrid devices offer-

## EVENT

## FDSOI Workshop in Japan

The University of Tokio, the SOI Consortium and Soitec are organizing a one day Workshop at the Komaba Research Campus of the University of Tokio on Saturday the 25th of September 2010 following the SSDM Conference focusing on the FDSOI ecosystem readiness.

This Workshop is co-organized by Dr. Ishimaru from Toshiba, Dr. Wakabayashi from Sony, Prof. Hiramoto from Tokio University, Dr. Mogami from Selene, Dr. Fukuma from the Semiconductor Industry Re-

search Institute Japan, Dr. Mazure and Mrs. B.Y. Nguyen from Soitec, and Dr. Méndez from the SOI Consortium.

Planar FDSOI technology offers today performance gain at very low power consumption in addition to a Vt variability reduction by 50-60% compared to bulk based processes. FDSOI technology enables low Vdd operation for logia and high density SRAM cells at sub-0.6V Vdd regime with excellent SNM and minimum cell size

ring a myriad of applications that were once the secure domain of function specific device, i.e. GPS systems and the new iPhone or Droid.

However, these adding these rich features can come with a cost: power consumption. SOI may provide new avenues to enable efficient design that provides optimal power management.

But how do you start to incorporate SOI design advantages into your next design? That's where

ARM, Cadence and partners as IBM, SOITEC, and the SOI Industry Consortium come into the picture. These companies began to actively start to work on reducing the barriers to entry of SOI technology by developing the design infrastructure critical to the fabless / foundry communities.

[Source: ARM Community Blogs]



## EUROSIO Network

**Thematic network on silicon on insulator technology, devices and circuits.**

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: [eurosoi@ugr.es](mailto:eurosoi@ugr.es)

The EUROSIO network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSIO aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

# CALENDAR

**- Third International Workshop on Compact Thin-Film Transistor (TFT) Modeling for Circuit Simulation (C-TFT)**

Tarragona, Spain.

July 2nd, 2010

**- ESSDERC ESSCRIC 2010**

Sevilla, Spain.

September 13th-17th, 2010

**- FDSOI Workshop**

Tokio, Japan

September 25th, 2010

**- 2010 IEEE International SOI Conference**

San Diego, California (USA)

October 11th-14th, 2010

**- 218 ECS Meeting**

Las Vegas, Nevada (USA)

October 10th-15th, 2010

**- EUROSIO 2011 Workshop**

Granada, Spain

January 17th-19th, 2011

**- CDE 2011**

Palma de Mallorca, Spain

February 8th-11th, 2011

**- Ultimate Integration on Silicon Conference (ULIS)**

Cork, Ireland

March 14th-16th, 2011

**- 219 ECS Meeting**

Montreal (Canada)

May 1st-6th, 2011