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**NEWS**

## GLOBAL INDUSTRY SURVEY RESULTS REFLECT STRONG INTEREST

### IN SOI FOR LOW POWER AT MAINSTREAM TECHNOLOGY NODES

The Global Semiconductor Alliance (GSA), an organization focused on accelerating the growth of the global semiconductor industry, and the SOI Industry Consortium, a group of leading companies throughout the electronics industry focused on accelerating silicon-on-insulator (SOI) innovation into broad markets, have announced the completion of a global study focused on SOI.

Over 100 semiconductor companies involved in the design of integrated circuits responded to the survey about their needs and perceptions of SOI. Eighty-seven percent of respondents indicated that they are interested in evaluating or are already using SOI, particularly for power savings at mainstream technology nodes starting with 90 nanometers. The survey also

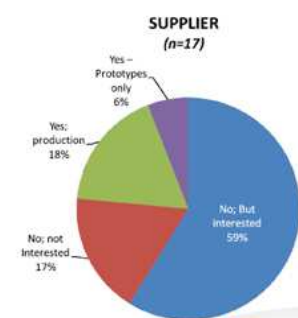
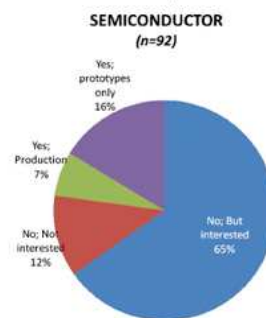
confirms the need to educate the market on available solutions, methodology and training across the global ecosystem, points that are being addressed by the SOI Industry Consortium.

“We are pleased to field the

study which will gauge perceptions of semiconductor companies on SOI technology,” said Jodi Shelton, GSA co-founder and executive director. “The collaboration on this survey with the SOI Industry Consortium provides us with a platform

#### Have you ever designed, supported or manufactured SOI chips?

87% of all respondents are interested or have used SOI



Source: GSA and SOI Industry Consortium 2008 Survey



## EUROSOI ANNOUNCEMENT

### Distinguished Lecturers list elaboration



EUROSOI+ is now elaborating a complete list comprised by experts in the

SOI field (fabrication, materials, devices, circuits, simulation, etc). This list will be specially useful to prepare all the training events in the next EUROSOI+ events.

See the EUROSOI web site for downloading the file that must be filled out and sent back before July 9th.

Do not hesitate to include yourself if you are considered as an expert in any specific SOI topic.

You can also:

- 1.- Include people that do not belong to the EUROSOI network or currently working out of Europe
- 2.- Widely broadcast this announcement to other colleagues out of the network.

from which we can determine industry education for the global community on SOI potential alternatives and benefits.”

“The results of the study show that there is an interest in SOI throughout the greater chip design, manufacturing and electronics community,” notes Horacio Mendez, executive director of the SOI Industry Consortium. “Respondents indicate that one of the main reasons they’re looking at SOI is to solve low-power challenges.”

[Source: SOI industry consortium & GSA]

## Semiconductor companies eye SOI advantages and obstacles

**“The SOI Consortium is actively working to resolve all of the issues that survey respondents cited as obstacles”, Méndez said.**

Fabless semiconductor suppliers are interested in silicon-on-insulator (SOI) because the technology allows power savings, but they remain concerned about costs, lack of silicon intellectual property (IP), and availability of EDA tools, according to a survey conducted by the Global Semiconductor Alliance (GSA) in cooperation with the SOI Consortium. The survey identified obstacles that must be overcome for wider SOI adoption.

The survey, available now on the GSA web site, compiled responses from 110 industry respondents holding positions such as CEO, CTO, director of engineering, and vice president of engineering. 94 are from semiconductor suppliers, design services providers, and systems companies. While several IDMs are represented, most of the semiconductor suppliers are fabless. 16 respondents are from supplier companies including IP, EDA, wafer foundries, equipment providers, and back-end service providers.

On the plus side, the survey found that 23 percent of respondents already use SOI. Another

64 percent don't use it today but are "interested." Power savings is seen as the most significant advantage, with many respondents willing to accept a higher total product cost to save power. Respondents expressed interest in SOI at conventional process nodes, such as 90 nm and 65 nm, in addition to advanced process nodes.

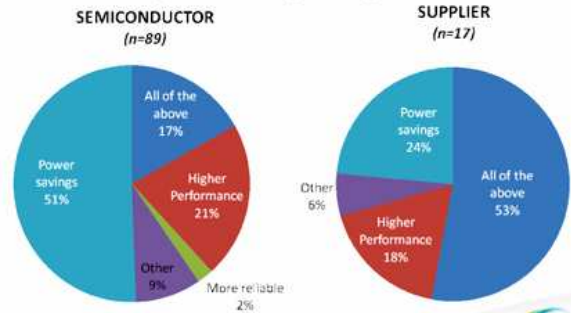
On the other hand, some respondents cited cost and lack of design knowledge as obstacles to SOI adoption. 56 percent were unsure whether their EDA tools are ready for SOI, and 12 percent said they are not, even though SOI advoca-

tes say that no significant tool changes are needed. Nearly half of the respondents noted that SOI intellectual property (IP) libraries are still inadequate or completely missing from the design flow today.

SOI, which electrically insulates the silicon active layer from the underlying substrate, has been adopted primarily by IDMs and used in fairly narrow niches such as high-end CPUs, and high-voltage and radiation-hard applications. The SOI Consortium is working to build an IP, EDA and foundry ecosystem that would

### What is the biggest potential advantage of using SOI for your business?

Semiconductor users indicate strong interest in power savings using SOI

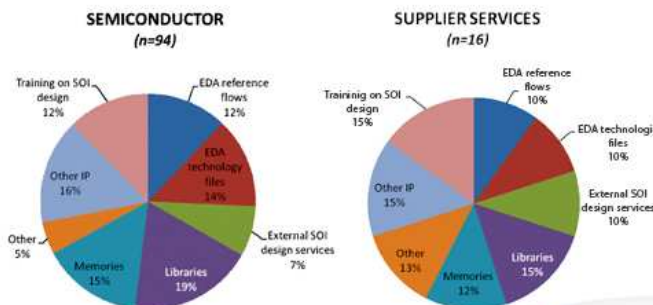


Source: GSA and SOI Industry Consortium 2008 Survey



### What is missing in your design flow for SOI?

IP topped the list for both users and suppliers



Source: GSA and SOI Industry Consortium 2008 Survey



broaden the adoption of SOI and bring it into the IC design mainstream.

The SOI Consortium is "actively working" to resolve all of the issues that survey respondents cited as obstacles, Mendez said. One approach is education. Mendez said that the consortium is organizing worldwide tutorials that show designers how to work with SOI. "There's a history effect," he said. "It's not tricky, it's just different. In a half day or so we can bring people up to speed."

[Source: SCDsource]

## NEWS

## Intel explores floating-body cells on SOI



At the 2008 Symposium on VLSI Technology in Hawaii, Intel Corp. revisited its research on floating-body cells (FBCs) for advanced cache designs in microprocessors.

The big question is whether Intel is finally endorsing silicon-on-insulator (SOI) technology, as the company will describe the world's smallest FBC-based planar device on SOI for possible use at the 15-nm node. In related paper, Intel is also expected to describe new adaptive circuit techniques for SRAM cache cells. Both technologies are in R&D and still in the lab, it was noted.

Waiting in the wings in the race towards

FBCs--or sometimes called floating-body RAMs (FB-RAMs)--is rival Advanced Micro Devices Inc. (AMD). Two years ago, AMD licensed an embedded FBC technology from Innovative Silicon Inc. (ISI).

For years, FBC has been touted as an alternative to conventional cache memory, because current capacitor-based technology is running out of gas. FBC is a candidate for increased memory density, compared to the standard six transistor (6T) cache memory that is used on all microprocessors today.

"In a standard DRAM, there is a capacitor and a transistor," according to ISI. "The capacitor stores the logic state, 1 or 0, and the transistor provides the rest of the circuitry access to the capacitor. To read a

DRAM memory cell, the transistor is turned on and the charge on the capacitor is allowed to flow onto a bitline, creating a small voltage which can then be detected."

Jeff Lewis, vice president of marketing at ISI (Santa Clara, Calif.), warned that there are some major issues cropping up with the capacitor in DRAMs, prompting the need for a new architecture. "Capacitor scaling is becoming almost impossible," Lewis said in a recent interview at the Design Automation Conference (DAC) in Anaheim, California.

[Source: *EE Times*]

## NEWS

## Selete Achieves 5 GHz Pulses on Silicon Photonics IC

Optical interconnects using an optical fiber and on-chip light guide are being developed as interconnects in servers, circuit boards, and on silicon chips, leveraging advantages such as higher speed transmission and lower power consumption. To that end, the Selete (Tsukuba, Japan) consortium said it has succeeded in transmitting a 5 GHz pulse waveform through a 4 mm light guide produced on a silicon IC. The consortium made the announcement at the recent Selete Symposium 2008.

The light guide serves as an optical interconnect using silicon as the base material, SiON as the core light guide, and

SiO<sub>2</sub> for the cladding layer. It connects to a light-emitting diode (LED) or laser diode made of a compound semiconductor. A Schottky barrier diode with a silver electrode is used as the photodetector. The light guide layer is produced on a silicon on insulator (SOI) wafer that is attached to the wafer holding the logic circuits, both with face-to-face electrodes.

Connections between the light-guide chip and logic IC are created with a gold-tin (Au-Sn) alloy, which allows for alignment of both electrodes. A previous proposal included optical connections between an optical interconnect wafer and circuit wafer, but that approach was deemed

unrealistic because of the difficulty of aligning both light guides.

In the technology developed by Selete, bump electrodes on the silicon wafer are connected to bumps on a light guide wafer, then the silicon substrate of the wafer with the light guides is etched off. The light guide consists of a SiON layer with a refractive index that is slightly higher than the surrounding SiO<sub>2</sub> cladding layer. The refractive index of the silicon layer is ~40% higher than that of SiO<sub>2</sub>. The silicon core has a higher transmission loss of 1-3 dB/cm, compared with 0.2-0.3 dB/cm for a SiON core.

[Source: *Semiconductor International*]

## EUROSUI NEWS

## First Call and Web site now available for the EUROSUI 2009 Workshop

EUROSUI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007) and Cork 2008, EUROSUI 2009 will be held at Chalmers, Göteborg. It

will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions. EUROSUI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

Information about the 2009 Workshop is now available at the Workshop web site

<http://chalmers2009.eurosoi.org>

Abstract submission and registration will be available in October.

CHALMERS



MC2  
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## NEWS

## CISSOID introduce a new High Temperature Logic Family



CISSOID is a Fabless Semiconductor company, leader in High Temperature

Electronics. They develop and sell Integrated Circuits (IC) designed for the highest reliability in the widest range of temperatures. Their products will operate at least from -55°C to +225°C. They have been tested from -200°C to +300°C. The reliability of CISSOID products is based on long years of experience in silicon technologies, design for reliability, assembly techniques and test.

CISSOID products are com-

monly used under extreme conditions and harsh environments, for example in demanding Oil&Gas, Aerospace and Automotive applications.

They enable exploitation of deep oil resources, energy savings in aircrafts and automobiles, optimal exploitation of geothermal resources, etc.

CISSOID proposes a portfolio of High Temperature standard products, such as Voltage Regulators, Voltage References, Clock Generators & Timers, Analog-to-Digital Converters, Amplifiers, High-Voltage MOSFET's and Drivers. Custom solutions can also be developed as an Appli-

cation Specific Monolithic IC (ASIC) or as a Hybrid multi-chip assembly solution.

Most of CISSOID's products are built on Silicon-on-Insulator (SOI), a fabrication process that offers tremendous advantages for High Temperature operation and high levels of radiation (Rad-Hard products). Cissoid's products inherit over 20 years of R&D activities in the field of SOI and was the very first company to exploit this technology.

[Source: CISSOID]

## EVENTS

## MIGAS International Summer School



This school is addressed to PhD students,

engineers and researchers coming both from the university and from industry of the semiconductors. Through a program based on lessons given by the best international scientists, the participants are given the opportunity of improving their knowledge on state of the art and future nanodevices.

Each session is focused on a different theme, and is managed by a different Scientific

Chair. This year, for its 11th session, MIGAS'08 has been focused on Nanoscale CMOS and Si-based Beyond CMOS Nanodevices.

The scientific programme for this edition was:

- Advanced materials, technology and characterization methods for nanoscale CMOS.
- Novel CMOS architectures.
- Beyond-CMOS Nanodevices.
- Innovative Memories.

This year the selected venue was Autrans, a reknown resort, dedicated to alpine and cross-country skiing in winter, and to tourism in summer, located in the Regional Natural Park of the Vercors mountains, 30 km away from Grenoble.



## EUROSIO Network

**Thematic network on silicon on insulator technology, devices and circuits.**

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: [eurosoi@ugr.es](mailto:eurosoi@ugr.es)

The **EUROSIO** network embraces a broad range of research areas related to **Silicon-On-Insulator** technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). **EUROSIO** aims at federating the existing research work on **SOI** topics and at providing an appropriate communication channel between academic groups and industrial production centres.

## CALENDAR

**- MIGAS International Summer School**

Autrans-Grenoble, France.

June 28th - July 4th, 2008

**- European School On Nanosciences & Nanotechnologies**

Grenoble, France.

August 24th - September 13th, 2008

**- Third SINANO Device Modeling Summer School**

Bertinoro, Italy.

September 1st - 5th, 2008

**- 38th European Solid State Device Research Conference and 34th European Solid State Circuits Conference**

Edinburgh, United Kingdom.

September 15th - 19th, 2008

**- 2008 IEEE International SOI Conference**

Hudson River Valley

New York, USA

October 6th - 9th, 2008

**- EUROSIO 2009 Workshop**

Chalmers University of Technology

Göteborg, Sweden

January 19th - 21st, 2009

<http://chalmers2009.eurosoi.org>