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Soitec's 300mm ultra-thin SOI prepped for 22nm applications



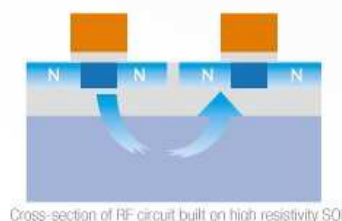
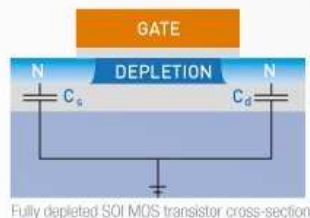
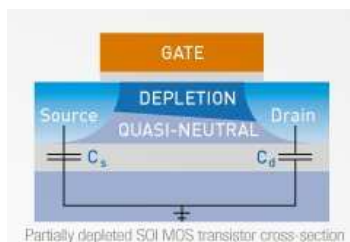
The Soitec Group has completed development and qualification of its 300mm ultra-thin SOI (UTSOI) wafer platform for use in supporting fully-depleted device applications on the industry's CMOS roadmaps for 22nm and beyond. The system is now ready to support mainstream ramp-up of fully depleted applications at the 22nm node, delivering a film thickness uniformity control of $\pm 5\text{\AA}$.

The UTSOI platform, which was introduced last year, has been undergoing process optimizations and customer qualifications that now enable customers to tailor the final SOI substrate to specific parameters. The company can now manufacture SOI with extremely thin top-layer silicon (20nm) to a thickness uniformity tolerance of $\pm 5\text{\AA}$ in high volume with high yields.

"On fully depleted SOI, we've demonstrated 25nm high-k metal-gate devices with matching characteristics far superior to those obtained on bulk silicon," reported Dr. Olivier Faynot, Director of

Advanced SOI technologies Development at CEA-Leti. "As it eliminates the need to dope the channel region, FD SOI solves threshold voltage (V_t) variability challenges at current and future nodes, while maintaining excellent Ion and Ioff characteristics and drastically reducing gate leakage current. With this uniform ultra-thin film SOI substrate, Soitec is delivering a solution for substantially improving V_t control of the CMOS device."

[Source: FabTech]



EVENTS

International Summer School on Advanced Microelectronics. MIGAS 2009

MIGAS Summer School is designed to foster and promote expertise in new, advanced topics of microelectronics. The aim of MIGAS is to offer every year a forum of detailed presentations on emerging topics of microelectronics.

It is also a unique opportunity for senior and junior researchers to update their knowledge in a very specific and emerging field. MIGAS brings together scientists from all over the world and from research institutes, universities, R&D small, medium and large

companies.

This year MIGAS Summer School was held from 20th - 26th June in Autrans-Grenoble, a renowned resort, dedicated to alpine and cross-country skiing in winter, and to tourism in summer, located 30 km away from Grenoble.

MIGAS 2009 topic was "Advanced SOI concepts: from materials to devices and applications" and lectures were given by world-class experts

(continues on page 2)

This year, for its 12th session, MIGAS'09 was focused on SOI concepts: from materials to devices and applications.

J-P. Colinge (Ireland), T. Hiramoto (Tokyo), A. Zaslavsky (USA), R. Schrimpf (USA), C. Fenouillet-

Béranger (STMicroelectronics), A. Asenov(Glasgow),O. Faynot, T. Ernst and B. de Salvo (LETI),

F. Gamiz (Granada), S. Cristoloveanu (Grenoble), etc.



MIGAS '09 - 12th session
SOI Concepts: From materials to devices and applications
 20 - 26 June 2009, Autrans-Grenoble, France



www.migas.inpg.fr



NEWS

Luxtera Announces Production Status of World's

First Commercial Silicon CMOS Photonics Fabrication Process



Luxtera, the worldwide leader in Silicon CMOS Photonics, announced its collaboration with Freescale Semiconductor as its foundry source to achieve production of the world's first commercial Silicon CMOS Photonics semiconductor manufacturing process. For a number of years, the companies collaborated on enhancing Freescale's SOI CMOS semiconductor fabrication process, at its Austin, Texas manufacturing facility, to add photonic circuit capabilities to an existing 130nm electronics manufacturing process. This new photonically enabled CMOS

fabrication process enables development and manufacturing of low cost Electro-Photonic Integrated Circuits (EPIC) bringing CMOS Photonics to mainstream markets ahead of the competition. Silicon CMOS Photonics is widely recognized as the key enabler of the next-generation of data-networking, computer, multi-core processor, and consumer electronics products.

Silicon CMOS Photonics technology enables design and manufacturing of optics and electronics on a single CMOS die. This process combines standard transistors for digital

and analogue electronic circuitry with passive nano-photon optical structures, as well as monolithic integration of active photonic device elements and enables direct fiber-to-the-chip attachments. The new fabrication process allows the production of integrated single chip transceivers for a multitude of applications. These CMOS Photonic transceivers offer better performance, increased reliability, and reduced power consumption of opto-electronic circuits at a fraction of the cost of traditional optical assemblies.

[Source: Business Wire]

These CMOS Photonic transceivers offer better performance, increased reliability, and reduced power consumption.

NEWS

Globalfoundries Demos 28nm, 32nm Wafers.



Globalfoundries, a joint venture between Advanced Micro Devices and Advanced Technology Investment Company, showed off its first wafers with logic produced using 32nm and 28nm process technologies. While existence of 32nm silicon-on-insulator wafers at Globalfoundries is hardly a surprise, bulk 32nm and 28nm wafers seems rather promising.

Globalfoundries is busy these days finding customers for itself as currently it has only one client: the parent company Advanced Micro Devices, which produces all of its central processing units (CPUs) at Globalfoundries and will also make its graphics processing units (GPUs) as well as core-logic sets using 32nm and 28nm bulk process technolo-

gies at Globalfoundries. The latter still needs to find more interested parties ahead of beginning to construct its third fab in New York, USA. No surprise, the firm brought its latest achievements to show at Computex Taipei 2009, the biggest technology trade-show in Asia.

At Computex, Globalfoundries demonstrated a wafer with six-core AMD Opteron "Istanbul" processors made using 45nm SOI process technology, a wafer with test chips produced at 32nm SOI node, a wafer with test chips processed at 32nm bulk node as well as a wafer with SRAM manufactured utilizing 28nm bulk fabrication process.

Since AMD's chief executive officer promised to ramp up processors using 32nm SOI process tech in the second half of 2010, it is hardly a revelation that Globalfoundries has test chips produced

using the technology. What is more surprising is that the company demonstrated its 32nm and 28nm bulk wafers, which implies that that it has been working on 32nm/28nm fabrication processes for quite a while. Earlier this year the company said it would be ready to accept orders for 32nm bulk production in late 2009. Early risk production using 28nm fabrication process is anticipated in the second half of 2010.

While Taiwan Semiconductor Manufacturing Company has yield issues with its 40nm process technology, demonstration of 45nm, 32nm and 28nm capabilities seems to be just what the doctor ordered for Globalfoundries to attract attention of the industry

[Source: X-bit labs]

NEWS

Infineon and LS Industrial Systems Form Joint Venture to Forge Ahead in Molded

Power Module Business for White Goods; Joint Venture to Accelerate Access to Power Module Market in Korea and Asia.



Never stop thinking

The Korean company LS Industrial Systems and Infineon Technologies AG announced the establishment of the joint venture LS Power Semitech Co., Ltd. which will focus on the development, production and marketing of molded power modules for white good applications. The establishment of the joint venture paves the way for Infineon and LS Industrial Systems to more rapidly access the promising market for energy efficient household appliances, such as washing machines, refrigerators and air conditioners, and also for other low-power consumer and standard industrial applications. The use of variable-speed motors to reduce the energy consumed by household appliances is growing in response to regulatory requirements and consumer demand. Concurrently, smart design of drive control electronics to make best use of these motors presents manufacturers with further opportunities for efficiency and savings.

LS Industrial Systems holds 54 percent and Infineon 46 percent of the joint ven-

ture with headquarters at LS Industrial Systems' site in the city of Cheonan which is located around 160 kilometers to the south of Seoul. Infineon will provide the joint venture with licenses to IP as well as technology and process know-how on its power module family CIPOS™ (Control Integrated Power System), and will transfer existing CIPOS backend manufacturing equipment from Regensburg, Germany. Both companies will closely cooperate in terms of marketing, international sales, and new product developments. LS Power Semitech expects to begin mass production for CIPOS modules by January 2010 in its Cheonan manufacturing site.

According to the current market report of the research firm IMS Research, Infineon holds the number one market position in semiconductor discretes and modules for power electronics having a 9.7 percent market share within the overall global market of US Dollar \$13.6 billion in 2007.

CIPOS power modules increase energy efficiency and reliability of home appliance motors

The CIPOS modules incorporate a three-phase inverter power stage with a SOI (Silicon-On-Insulator) gate driver, boot strap diodes and capacitors, and auxiliary circuitry in a compact, high-performance, fully isolated package. Based on a combination of Infineon's leading-edge TRENCHSTOP™ IGBT (Insulated Gate Bipolar Transistor) and emitter controlled diode technology, they eliminate as many as 23 discrete components compared to a design based on discrete components. The CIPOS modules also offer the industry's lowest junction-to-case resistance, which increases output current by up to 20 percent compared to other available modules.

The CIPOS family today comprises various members including modules for three-phase IGBT inverters for the voltage classes 5V or 3.3V with and without fault detection, for three-phase IGBT inverters with closed common emitter and for two-phase IGBT inverters for switched reluctance drives. The CIPOS modules are available in a RoHS-compliant single-in-line package that is best-suited for washing machine applications.

[Source: Infineon]

NEWS

SOI Industry Consortium reinforces its academic and research

support; three more prestigious universities join



The SOI Industry Consortium, an international group

aimed at accelerating broad adoption of silicon-on-insulator (SOI) materials technology across semiconductor markets, announced that it is reinforcing its academic and research support with the additions of three prestigious universities at the forefront of SOI applied research. Stanford University, University of California, Berkeley and Ritsumeikan University, Kyoto, Japan have all joined the consortium as academic members.

"We are very pleased to welcome Stanford, U.C. Berkeley and Ritsumeikan University. With these additions, we are expanding our excellent eco-

system of prestigious academic and research support," says Horacio Mendez, Executive Director of the SOI Industry Consortium. "Our members in academia are key contributors in both basic and applied SOI research. Together, we can facilitate cooperation with industry and other research organizations, helping to accelerate the use of SOI in both emerging and established application fields. Conversely, academia is our gateway to the future, providing our industry with researchers and engineers who have a strong grounding in the use and advantages of SOI."

The SOI Industry Consortium will continue promoting cooperation between commercial members and

academia and research institutes. Representing leaders spanning the entire electronics industry infrastructure, the SOI Industry Consortium's membership now counts seven academic members and research institutes worldwide. The others include Tyndall Institute, "Université Catholique de Louvain" (UCL), as well as IMEC, and Leti. The group's expertise covers key areas such as ultra-low power applications, MEMS, advanced CMOS, Fully Depleted (FD) SOI, FinFETS, photonics, analog, SOC and RF applications.

[Source: SOI Industry Consortium]

"Together, we can facilitate cooperation with industry and other research organizations, helping to accelerate the use of SOI in both emerging and established application fields" says Horacio Méndez.

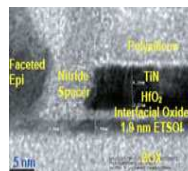
NEWS

Thin SOI Devices Shine at VLSI Symposium

IBM researchers went to the Symposium on VLSI Technology in Kyoto, Japan, to present a fully depleted CMOS process integration scheme for extremely thin silicon-on-insulator (ETSOI) devices, aimed at the 22 nm node and beyond.

The IBM process flow avoids implant steps, as does another thin buried oxide (BOX) SOI process flow presented at the symposium by researchers from the Hitachi Central Research Laboratory (Kokubunji, Japan). The Hitachi team said that in conventional CMOS on thin BOX substrates, halo implantation can cause damage to the gate oxide, especially at the gate edge. For the ultrathin BOX technology, which Hitachi calls Silicon on Thin BOX (SOTB), ion implantation was avoided to prevent damage to the oxide. Hitachi created SRAM devices that operated at 0.6 V, and said

the ability to reduce the operating voltage was due to better control of the threshold voltage variations through the use of the thin buried oxide.



The IBM team developed prototype devices using its high-*k*/metal gate technology.

The source/drain (S/D) and extensions were doped by an in situ epitaxial process, resulting in an implant-free flow to successfully reduce series resistance below 200 $\Omega/\mu\text{m}$. "A zero-silicon-loss process was developed to eliminate loss of the thin SOI layer during gate and spacer processes, enabling structural demonstration of sub-2 nm ETSOI," the IBM team reported.

Even without strain boosters, the IBM paper claimed a "remarkable" pFET drive current of 550 $\mu\text{A}/\mu\text{m}$ with a 6 nm SOI channel and a 25 nm

physical gate length. A 15% reduction in parasitic capacitance was achieved by a faceted raised source/drain (RSD). "Excellent electrostatics and small device dimensions render ETSOI devices suitable for the 22 nm node and beyond," the IBM team reported.

IBM's VLSI symposium presentation said fully depleted SOI with an extremely thin body has advantages, including superior control of the short channel effect with negligible dopant fluctuation. However, ETSOI poses new challenges such as extension engineering, high series resistance, increased parasitic capacitance and nearly zero tolerance of silicon loss. The performance of the pFET is of particular concern, because the strain techniques that work well for pFETs in conventional CMOS, such as embedded silicon germanium (eSiGe) stressors, are not possible with ETSOI.

[Source: Semiconductor International]



EUROSIO Network

Thematic network on silicon on insulator technology, devices and circuits.

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

The EUROSIO network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSIO aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

CALENDAR

- European School On Nanosciences & Nanotechnologies

Grenoble, France.

August 23rd - September 12th, 2009

- 216th ECS Meeting

Vienna, Austria.

October 4th - 9th, 2009

- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference

Athens, Greece.

September 15th - 19th, 2009

- 2009 IEEE International SOI Conference

Foster City, USA.

October 5th - 8th, 2009