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EUROSOI

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HIGHLIGHT NEWS

Cadence Announces Comprehensive SOI Design Hub

 Cadence Design Systems, Inc., the leader in global electronic design innovation, introduced the Cadence® SOI Design Hub, a new Web portal that lowers the barriers to adopting silicon-on-insulator (SOI) technology through comprehensive silicon-proven design enablement solutions and services. The SOI Design Hub is aimed at reducing SOI adoption start-up costs, cutting time to market for SOI intellectual property (IP), and improving design quality.

Cadence has been working with IBM, the leading SOI foundry, and with ARM to deliver methodologies, reference flows, IP access and services for SOI design. This includes the recent delivery of a 45-nanometer SOI SerDes receiver. Cadence also recently announced a joint development agreement with IBM to develop complex IP, including SOI designs, as part of the Cadence open integration platform. Forty-five-nanometer SOI technology offers up to 30 percent performance improvement or 40 percent power reduction when compared to the industry-standard bulk CMOS technology.

The Cadence open integration platform is a key component of the EDA360 vision, which, among other things, helps integrators close the profitability gap by providing new capabilities for IP creation, selection and integration.

"Cadence and IBM have collaborated for several SOI process generations to deliver silicon-proven methodology to our mutual customers," said Mark Ireland, vice president, Semiconductor Products and Services,

IBM. "Providing this proven technology and Cadence services expertise is an excellent way to help customers in adopting SOI technology."

Through the SOI Design Hub, Cadence now offers three new solutions: An SOI IP porting service, where Cadence Services migrates analog, digital, and mixed-signal IP blocks to an SOI process technology, and delivers a self-contained macro that will integrate smoothly with the target design environment; turnkey design services, where customers can outsource any aspect of their design to the SOI design-experienced Cadence team; and a software-as-a-service (SaaS) offering with a complete do-it-yourself IP porting environment that provides access to a production-proven Cadence design environment within a secure IT infrastructure.

"As adoption of SOI technology continues to grow it is important to have a central point for accessing design enablement tools and IP to accelerate the design cycle and industry adoption," said John Heinlein, vice president of marketing, ARM, Physical IP division. "The Cadence SOI Design Hub,

coupled with ARM physical and processor IP, provides engineers a silicon-proven route for leveraging this advanced technology to deliver high-performance, low-power consumer devices while reducing design risk and cost."

"We've been working diligently with IBM and ARM to make SOI adoption easier for our customers and enable them to benefit from this advanced technology," said Vishal Kapoor, vice president of product management at Cadence. "The new SOI Design Hub will help realize designs for those interested in leveraging the power and performance benefits of this technology with the solutions and services they need to ensure success."

"This innovative offering by Cadence provides a range of new options for companies to leverage the power efficiency and integration benefits of SOI technology in their products," said Horacio Mendez, executive director of the SOI Industry Consortium. "The SOI Design Hub is a significant addition to the SOI design chain for the electronics industry."

[Source: Cadence]

ANNOUNCEMENT Coming up: EUROSOI 2011



Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada,

Andalucía (Spain) from **January 17th to January 19th**. It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

<http://granada2011.eurosoi.org>

NEWS

Startup proposes SOI JFETs for low power



SuVolta Inc. (Los Gatos, Calif.), a

startup formerly known as DSM Solutions Inc., has revealed some details of the company's plan to achieve low power IC operation through the use of complementary junction FET technology.

Ashok Kapoor, CTO of SuVolta, made a presentation at the 2010 CMOS Emerging Technologies Workshop held in Whistler, British Columbia, May 19 to 21. In this case CMOS stands for communications, Microsystems, optoelectronics and sensors. Kapoor's presentation was variously entitled "VLSI with complementary JFET" and "JFET technology for very low power." The lateral junction FET differs from a MOSFET in that it uses a reverse-biased p-n junction to separate the gate from the body of the transistor, rather than an insulation layer. Also its channel doping is the same as the doping of its source and drain creating similarities in operation to proposed junction-less nanowire transistors.

Kapoor was part of the team of

founders that formed DSM Solutions in 2005. The company has raised \$25 million since then and taken on to its board of directors Bill Joy and Andy Rappaport to represent the interests of venture capital firms Kleiner Perkins Caufield & Byers and August Capital, respectively. SuVolta raised \$3 million in December 2009, by which time the company had changed its name to SuVolta and Bruce McWilliams, former chairman, president and CEO of chip packaging company Tessera Technologies Inc. (San Jose, Calif.), had joined as CEO. The company has been granted a number of patents on the use of JFET technology for low-power logic, memory and signaling.

In his Whistler presentation Kapoor proposed the use of a double-gated JFET as it has a near-ideal sub-threshold swing. He gave measurements for NFET and PFET structures built with a 60-nm gate.

Kapoor also showed results for 99-stage ring oscillator built with complementary JFETs on bulk silicon. He also discussed the drawbacks of high p-well capaci-

tance and the area penalty incurred to isolate transistors for JFETs implemented in bulk silicon. Kapoor's proposed solution is to build complementary JFETs on a silicon-on-insulator (SOI) substrate.

In his summary to the Whistler presentation Kapoor said: "Subsequently, functional logic circuits made with JFET on SOI have also been demonstrated." He concluded: "JFET operation has been simulated for channel length below 20-nm with reasonable Ion/Ioff ratio for voltage supply of 0.5V, making it a candidate for scaling to shorter dimensions."

Jeff Lewis, recently-appointed vice president of marketing and business development, said SuVolta is "developing a variety of technologies and methodologies for significantly lowering semiconductor power consumption." Lewis also told EE Times: "We are not going to make our own chips; instead we will make the technology available to others so they may include it in their own products."

[Source: EETimes]

NEWS

Kilopass Announces Embedded Logic NVM for SoCs



Kilopass Technology Inc., a

leading provider of semiconductor logic non-volatile memory (NVM) intellectual property (IP), announced **Gusto**, the industry's first and only 4 megabit (Mb) one-time programmable (OTP) NVM IP. Gusto is the only NVM IP large enough to store the firmware and boot code traditionally stored in external serial-flash and EE-PROM chips. It is ideal for cost-,

power- and form factor-sensitive applications, including mobile application processors and multimedia processors, as well as for high-security applications such as mobile banking and conditional access. Kilopass has successfully taped out Gusto 40nm test chips at three leading foundries – IBM, TSMC, and UMC. Initial silicon data is available now, and qualified proven silicon will be available later this year.

Gusto eliminates the limitations of traditional embedded NVM

technology, including poor scalability to advanced processes and capacity limitations of less than 128Kb. Moreover, it does not require the complex manufacturing technology changes generally required by today's traditional embedded NVM. Instead, using standard CMOS manufacturing processes, Gusto scales to meet embedded NVM size and complexity challenges that grow exponentially as SoCs migrate to 40nm, and soon 28nm.

[Source: ChipDesign]

SuVolta is "developing a variety of technologies and methodologies for significantly lowering semiconductor power consumption.", said Lewis.

Gusto Delivers 4Mb One-Time-Programmable Ultra-Secure Storage for Consumer and Mobile applications .

NEWS

TEGAL receives repeat order for TEGAL 4200 SE Cluster tool Silicon drie process

module

tegal Tegal Corporation, an innovator of specialized production solutions for the fabrication of advanced MEMS, power ICs and optoelectronic devices, announced it has received an order for an additional Tegal 4200 SE™ DRIE cluster tool process module from a leading EU-based supplier of MEMS and Power IC devices. The Tegal 4200 SE DRIE process module will be shipped and installed at the customer's site in the next fiscal quarter, and will add to the customer's overall production capacity for high volume manufacturing of MEMS and Power IC devices.

The Tegal 4200 SE cluster tool silicon DRIE process module order from this repeat Tegal DRIE customer follows the successful installation, process qualification, and sustained use of silicon Deep Reactive Ion Etch processes on the

customer's first Tegal 4200 SE cluster tool PM.

"Our customer is known for their technological leadership in the MEMS and Power IC markets, and we see this repeat order as confirmation of the Tegal silicon DRIE tool's superior performance in high volume manufacturing," said Yannick Pilloux, DRIE Product Manager at Tegal Corporation. "We believe that our DRIE process modules are the most reliable and most advanced on the market and, as this repeat order shows, we have been able to meet our customer's demanding technical requirements for silicon DRIE cluster tools, while providing excellent value along the way."

The Tegal 4200 SE™ is an advanced, world-class cluster tool system dedicated to Deep Reactive Ion Etch applications. Featuring an inductively coupled plasma etch reactor and magnetic plasma confinement, the tool can run Tegal's patented

SHARP – Super High Aspect Ratio Process, achieving etched feature aspect ratios of >100:1 in production environments. The Tegal 4200 cluster tool can be configured with up to 4 process modules, and 2 cassette modules, for High Volume Manufacturing applications for the most frequently used materials in MEMS and semiconductor device fabrication: Silicon (Si), Silicon On Insulator (SOI), and Silicon Dioxide (SiO2)

Tegal silicon DRIE tools are presently employed in numerous research and development laboratories throughout the world, engaging in both commercial and academic research programs, and are also found in MEMS foundries and other dedicated commercial High Volume Manufacturing lines world-wide.

[Source: Tegal]

NEWS

BroadPak joins SOI Industry Consortium



The SOI Industry Consortium, aimed at accelerating silicon-on-insulator (SOI) innovation across broad markets, announced that BroadPak has joined the worldwide organization. BroadPak is a premier provider of semiconductor package design and development services. The addition of BroadPak, with its unique silicon-package co-design methodology, ex-

pands opportunities for SOI chip developers to reduce product cost and improve chip and system performance without impacting chip development schedules.

"BroadPak brings its expertise in advanced high-performance, high pin-count package design and test to the SOI community," said Farhang Yazdani, president and chief technical officer of Broadpack.

[Source: Soi Industry Consortium]

REMEMBER:

Early registration deadline for ESSDERC ESSCIRC 2010 is July 28th

ANNOUNCEMENT

Finalizing details for ESSDERC / ESSCIRC 2010 in Sevilla



The 40th **European Solid-State Device Research Conference (ESSDERC)** and the 36th **European Solid-State Circuits Conference (ESSCIRC)** will be held in Sevilla on 13 - 17 September 2010.

The aim of the ESSDERC and the ESSCIRC conferences is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits.

ESSDERC and its sister conference ESSCIRC are governed by a single Steering Committee. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts, and circuit and system designers. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC will share Plenary Keynote Presentations and Joint Sessions bridging both



Detail of the Cathedral in Sevilla.

communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions.

NEWS

Freescale Extends QorIQ Family with Quad-Core P3

Platform Optimized for Low Power



Freescale Semiconductor is expanding the performance range of its QorIQ™ communications processor product lines with the introduction of the quad-core QorIQ P3 platform. The new P3041 processor offers an advanced feature set leveraging Freescale's P4 platform technology and optimized for low power, enabling increased system performance and improved overall power consumption.

The new QorIQ P3041 expands the reach of Freescale's P4 platform into lower power applications. Manufactured in 45nm silicon-on-insulator process technology, the P3041 offers optimal integration and new intellectual property that delivers improved functionality for end products. The P3041 processor integrates four e500mc cores based on Power Architecture® technology running up to 1.5 GHz at less than 12 watts, and delivers

about 2.5 DMIPS/MHz. Key features include a three-level cache hierarchy for optimized latencies, a hardware hypervisor for robust support of multiple operating systems within the device, a trusted boot architecture to ensure code is not tampered with or reverse engineered, efficient data path handling, and improved Serial RapidIO and SATA IP.

[Source: EDACafé]

The P3041 offers optimal integration and new intellectual property that delivers improved functionality for end products

NEWS

IBM 'fab club'

aligns 28-nm process, jabs rival

Four companies in IBM Corp.'s "fab club"—IBM, Samsung, GlobalFoundries and STMicroelectronics—said that they are in collaboration to "synchronize" the production of chips, based on its previously-announced, 28-nm low-power process.

The group will begin shipping 28-nm wafers starting by the later part of 2010. IBM's group has also come out of its shell and launched a subtle verbal attack on the rival foundry camp, reportedly Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC).

The group did not mention TSMC by name, but the Taiwan foundry giant has been critical of the high-k technology implemented by IBM's group. IBM's 28-nm process is based on a high-k/metal-gate scheme, built around a gate-first technology.

In contrast, TSMC uses the rival gate-last technology in its high-k technology. Members of IBM's fab club defended its technology, saying that it's superior over compe-

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NEWS

SOI Industry Consortium confirms

new board members



The SOI Industry Consortium, a not-for-profit organization aimed at accelerating innovation and adoption of energy-efficient silicon-on-insulator (SOI) technology across the electronics industry, announced new additions to its board of directors: Michael J. Cadigan, general manager, IBM Microelectronics

Systems & Technology Group, as the new board chair; Simon Segars, executive vice president and general manager, Physical IP Division, ARM Ltd.; and Laurent Maller, chief executive officer of CEA-Leti, as its new treasurer.

[Source: SOI Industry Consortium]

titive offerings.

In any case, leading-edge foundries are rushing to bring their latest and greatest processes to the market—and for good reason: The IC market is hot and the outsourcing specialists hope to capitalize on the up cycle. Many of the foundries have also boosted their capital spending and launched marketing campaigns to gain mindshare.

At present, leading-edge foundries are shipping their 45-/40-nm pro-

cesses, which do not include high-k and metal gates. All are gearing up to ramp their 32- and/or 28-nm processes, which brings the foundries into the high-k era.

In the foundry space, IBM's fab club, TSMC and UMC have separately announced 28-nm processes based on high-k. IBM's group and TSMC claim to be the leaders in the segment.

[Source: EETimes]



EUROSIO Network

Thematic network on silicon on insulator technology, devices and circuits.

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

The **EUROSIO** network embraces a broad range of research areas related to **Silicon-On-Insulator** technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). **EUROSIO** aims at federating the existing research work on **SOI** topics and at providing an appropriate communication channel between academic groups and industrial production centres.

CALENDAR

- **International Symposium on Circuits and Systems. ISCAS 2010**

Paris, France.

May 30th - June 2nd, 2010

- **218 ECS Meeting**

Las Vegas, USA.

October 10th - 15th, 2010

- **Third International Workshop on Compact Thin-Film Transistor (TFT) Modeling for Circuit Simulation (C-TFT)**

Tarragona, Spain.

July 2nd, 2010

- **EUROSIO 2011 Workshop**

Granada, Spain.

January, 2011

- **ESSDERC ESSCRIC 2010**

Sevilla, Spain.

September 13th - 17th, 2010

- **2010 IEEE International SOI Conference**

San Diego, California (USA)

October 11th-14th, 2010