



HIGHLIGHT FEATURE

FD-SOI: The Substrates Are Ready

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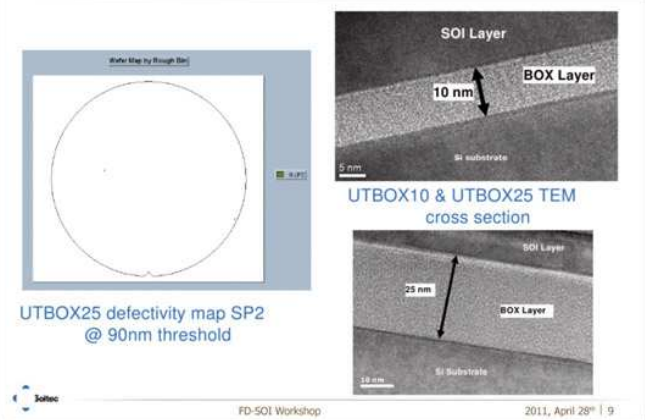


Olivier BONNINI
Soitec

At the most recent SOI Consortium FD-SOI workshop, Soitec gave a presentation on FD-SOI substrate readiness. Here are some of the highlights.

The roadmap for FD-SOI architectures requires SOI wafer structures with ultra-thin top silicon and ultra-thin insulating BOX (Xtreme SOI™). Using our industry-standard Smart Cut™ technology, Soitec is ramping these wafers in production for high-volume manufacturing that meet all the current requirements for the 20/22nm node.

UTBB Substrate is Real



For this node, the thicknesses of the target structure are 12nm silicon and 25nm BOX to accommodate body bias strategies. The

industry is referring to these wafers as UTBB, for ultra-thin body bias.

For manufacturing such wafers, the main challenges were ensuring that both the top silicon and BOX respected the extremely stringent requirements for thickness uniformity and site flatness.

The reason for this is that for undoped FD-SOI transistors, thickness uniformity is the critical element in controlling threshold voltage (V_t) variation.

By fine tuning of elementary process steps in our Smart Cut process, we are able to produce UTBB wafers. The following illustrations highlight how we do it.

[Olivier Bonnini is Product Integration Manager at Soitec]



Thickness is within 4.1 Angstroms.



Wafers for nodes several generations away are currently sampling.



Ensuring ultra-thin silicon and BOX layers requires tuning the Smart Cut process oxidation and cleaning steps.



To control uniformity at the atomic level requires continual wafer-to-wafer and on-wafer control, feedback/feedforward and careful tuning of the Smart Cut process's oxidation, ion implantation, splitting and finishing steps.

FEATURE

Get Smart



Adele HARS
Advanced Substrate News

ST's latest BCD shows how SOI yet again enables huge reductions in power consumption.

What if you had to reduce power dissipation by 40x?

That's exactly the task that fell to ST, under an EU program called Smart Power Management.

At the recent ISPSD (International Symposium on Power Semiconductor Devices and ICs) conference, STMicroelectronics and partners (GE Vingmed Ultrasound and Sintef) presented a paper on how they did it, using ST's latest SOI-based Smart Power technology.

Paola Galbiati, ST's Director of the BCD Technology Line, Technology R&D covered this project in her recent ASN article, "Smart Power Saves Power".

As she notes, ST has been solving critical power management challenges with SOI-BCD (Bipolar-CMOS-DMOS) processes for almost a decade now. The technology they developed under the SmartPM project is a next-

generation variation of their BCD smart power technology, combining SOI with 0.16-micron lithography.

While the technology is applicable to chargers for electric car batteries, the first proof point was done for ultrasound probes.

The trend toward 3D ultrasound using internal probes imposes draconian limits on power. After all, you can't have the doctor putting something hot and bulky down your throat in order to image your heart.

2D probes typically have a couple hundred channels, consuming a total of about 3W of power. But for advanced 3D imagery, thousands of channels are needed – with total power consumption cut to 1.8W: about 40 times less.

This was not possible with discrete components, but it is with technology like ST's SOI-BCD, which enables chip designers to combine high-density logic circuitry (1.8V and 3.3V CMOS) with full dielectric isolation and a component portfolio. They can include power MOSFET transistors that can operate up to 300V, low noise devices and high-value resis-

tors, leading to ASICs that couldn't be implemented using conventional bulk-silicon substrates.

ST's now got first silicon, so product design engineers can start planning a whole new generation of cutting edge solutions.

Add this to the fast-growing list of SOI-enabled game changers.

[Source: Advanced Substrate News]



Transesophageal probes, which are inserted into the esophagus via the throat, send a beam across the esophageal wall to image the heart structures. The constraints on space and power consumption for the embedded electronics are extremely stringent.

"technology like ST's SOI-BCD [...] enables chip designers to combine high-density logic circuitry (1.8V and 3.3V CMOS) with full dielectric isolation and a component portfolio", says Hars

CONFERENCE

2011 IEEE International SOI Conference.



Submission period for 2011 International SOI

Conference was closed at the end of **May, 2011**.

For over 35 years the IEEE International SOI Conference has been the premier meeting of engineers and scientists dedicated to current trends in Silicon-on-Insulator technology. Sponsored by the IEEE Electron Devices

Society, the conference traditionally provides a forum for open discussion in all areas of SOI technologies and applications as well as the introduction of new developments presented in original papers presented at the technical sessions.

More information as well as a detailed programme can be found at the conference site:

<http://www.soiconference.org>



Tempe Mission Palms Hotel and Conference Center

NEWS

Freescale's new QorIQ™ P2041 quad-core processor on 45nm SOI



Freescale's new QorIQ™ P2041 quad-core processor on 45nm SOI for security and other networking equipment delivers up to 10 Gb/s performance and operates at 12W typical power.

Freescale Semiconductor is making enterprise class features for security networking equipment available to small-medium businesses (SMB) with its new QorIQ™ P2041 quad-core processor. Targeting unified threat management (UTM) security appliances, the P2041 delivers up to 10 Gb/s performance in smaller, less expensive form factors such as the 1U chassis.

The P2041 combines high-end multicore processing engines with features such as hardware virtualization, cryptography and deep packet inspection technology in a single-chip solution. This integration reduces costs compared to UTM appliances based on common two- and three-chip

models. In addition, the energy-efficient P2041 operates at 12W typical power.

"The P2041 integrates optimal processing performance with high-end features such as broad I/O scalability and advanced deep packet inspection functionality," said Danny Mulligan, director of marketing for Freescale's Networking Processor Division. "The processor offers UTM equipment manufacturers a quad-core, low-power solution with a mix of enterprise-like features and capabilities at SMB price points and form factors."

The P2041 is pin-compatible with Freescale's P2040 device and software-compatible with members of Freescale's range of QorIQ platforms from P1 to P5 levels. This allows customers to easily scale their end solutions and leverage their software investment across a broad array of products.

In addition to UTM systems/security appliances for SMB, the P2041 is ideal for

applications such as LTE base station network interface cards (NICs), single-chip enterprise router solutions, multi-function printers, data centers, application delivery controllers, storage equipment, factory automation technology and iSCSI and switch management controllers.

Market-leading ODM Lanner, Inc. has adopted Freescale's P2041 device in its new MR-630 UTM solution. Demonstrating the outstanding performance and power profiles attainable with the P2041, the Lanner MR-630 appliance delivers 10 Gb/s processing power in a 1U chassis, hardware accelerated encryption capabilities and deep packet inspection. It also supports virtualization for application consolidation and in-service upgrades.

[Source: Freescale Semiconductor]

FEATURE

FD-SOI update



Horacio MÉNDEZ
Executive Director, SOI Industry Consortium

Data indicates that fully-depleted (FD) SOI offers an ideal combination for achieving ultra-low-power, high-performance and cost-effective manufacturability. Companies in the SOI Consortium are working together on furthering the development and technology evaluations.

February Results at the Circuit Level

A group of companies within the SOI Consortium (ARM, Global Foundries, IBM, SOITEC, ST and Leti), have collaborated to simulate the impact of using FD SOI on an ARM M0 Cortex core. These results were made available in a press release in February 2011 and are described below:

Benchmarking circuit: ARM Cortex M0 processor core

- Logic only (no memory)
- 30k Gates
- Usual Arm core used to test advanced

technologies

- P&R circuit using standard EDA tools

Target technology:

• 20nm FD-SOI

Results: Impressive advantage at low Vdd

VDD	LP Bulk Generation N	LP Bulk Generation N +1	FD SOI Generation N +1
	Normalized frequency to 1	Typical % performance improvement	Additional % performance improvement
0.7	1	+25%	+80%
0.8	1	+25%	+40%
0.9	1	+25%	+25%

NEWS

NXP has introduced the GreenChip SSL4101T controller IC for Solid State LED lighting power supplies

NXP has introduced the GreenChip SSL4101T controller IC for Solid State LED lighting power supplies. Based on SOI, its industry-leading performance includes Total Harmonic Distortion (THD) of less than

20 percent, a high Power Factor (PF) of .99, and high efficiency of 94 percent.

[Source: Advanced Substrate News]



EUROSIO Network

Thematic network on silicon on insulator technology, devices and circuits.

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

The **EUROSIO** network embraces a broad range of research areas related to **Silicon-On-Insulator** technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). **EUROSIO** aims at federating the existing research work on **SOI** topics and at providing an appropriate communication channel between academic groups and industrial production centres.

CALENDAR

- ESSDERC ESSCRIC 2011

Helsinki, Finland

September 12th-16th, 2011

- IEDMS 2011 : International Electron Devices and Materials Symposium 2011

Taipei, Taiwan

November 17th-18th, 2011

- 2011 IEEE International SOI Conference

Tempe, Arizona (USA)

October 3rd-6th, 2011

- 221 ECS Meeting

Seattle, Washington (USA)

May 6th-11th, 2012

- 220 ECS Meeting

Boston, MA (USA)

October 9th-14th, 2011

- 5th International Workshop on Compact Thin-Film Transistor (TFT) Modeling for Circuit

Tarragona, Spain

November 9th-10th, 2011