

THEMATIC NETWORK  
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# EUROSIO

# Newsletter

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## HIGHLIGHT NEWS

## GLOBALFOUNDRIES Opens for Business

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**G**lobalFoundries, a new leading-edge semiconductor manufacturing company formed by a joint venture between AMD and the Advanced Technology Investment Company (ATIC), announced its official launch and outlined plans to drive profound change and expand opportunities in the semiconductor industry. GlobalFoundries is led by an experienced semiconductor management team, including CEO Doug Grose, formerly senior vice president of manufacturing operations at AMD, and Chairman of the Board Hector Ruiz, formerly executive chairman and chairman of the board at AMD. The Company is the only U.S. based global semiconductor foundry and commences operations with approximately 2,800 employees worldwide with headquarters in Silicon Valley.

"The launch of GlobalFoundries represents a historic day for our industry, one which will permanently change the market landscape by launching the world's first truly global foundry services provider," said Doug Grose, Chief Executive Officer of GLOBALFOUNDRIES. "With two committed joint venture partners providing strong technology and capital resources, our company brings a unique set of global capabilities to the market that will enable our customers to fully unlock their potential to innovate."

GlobalFoundries will service the manufacturing needs of AMD and will also offer an expanded roadmap of technologies to third-party customers through its high-volume, global foundry services. This means that for

the first time, early access to volume chip production using leading-edge technologies will not just be limited to only high-end microprocessor makers.

"As consumers move to increasingly smaller and more power-efficient devices we need to remain aggressive in our technology development and ensure we have the right foundry partners to get those products to market," said Simon Segars, Executive Vice President and General Manager, ARM. "Through the integration of our own processor and physical IP and our industry collaboration activities we continue to facilitate the adoption of next-generation consumer electronics. We look forward to working with GlobalFoundries as we explore their advanced technology capabilities on the ARM platform to support the growing needs of our customers around the world."

To meet the long-term needs of the industry, GlobalFoundries is proceeding with plans to expand its Dresden, Germany, manufacturing lines by bringing a second

300mm manufacturing facility with bulk silicon capabilities online in late 2009. The Dresden cluster will be re-named Fab 1 with Module 1 initially focused on production of high-performance 45nm Silicon-on-Insulator (SOI) technology, and Module 2 transitioning to 32nm bulk silicon capabilities.

In addition to Fab 1 the company also plans to begin construction on a new state-of-the-art 32nm and smaller features, \$4.2B manufacturing facility at the Luther Forest Technology Campus in Saratoga County, NY, in 2009. This new facility will be named Fab 2 and is expected to create approximately 1,400 new direct jobs and more than 5,000 indirect jobs in the region. Once operational, Fab 2 will be the only independently-managed, advanced semiconductor manufacturing foundry in the United States, bucking the trend of manufacturing industries leaving the U.S.

GlobalFoundries is jointly owned by AMD and ATIC

[Source: GlobalFoundries]

## ANNOUNCEMENT

## Tutorial Section on

## the EUROSIO Website Complete

 Following the efforts that the EUROSIO team is making to improve its work and with the dedication that has been shown thus far, the new tutorial section is now complete containing the different tutorials held since the first EUROSIO Works-

hop in Granada in 2005.

The different tutorials are organized according to their dates and places and a search engine by years has been also developed. For further details take a look at:

<http://www.eurosoi.org/tutorials.asp>

## NEWS

## Green tech drives ICs beyond silicon



The green technology era will drive

semiconductor innovations in and beyond silicon across a wide variety of applications, according to Rene Penning de Vries, chief technology officer of NXP Semiconductors in a keynote at the International Solid State Circuits Conference (ISSCC) here.

"The electronics industry has grown by focusing on productivity and using power as a resource in a formula that has resulted in tremendous success in consumer electronics, computing and communications," said De Vries.

"Now the equation is different, and the industry has a role to play optimizing power use," he said.

Traditional shrinks in CMOS process technology are not sufficient

to meet all the needs of this green era. The new dynamics will drive a wide range of innovations beyond the traditional shrinks in CMOS technology, requiring new kinds of materials and processes, he said.

For example, the pursuit of power-efficient high-volt circuits "silicon-based solutions are coming to an end," De Vries said. "The next breakthrough will be based on new materials and gallium nitride is one of the promising ones," he said

In another example, he briefly described a new silicon-on-insulator circuit to drive a compact florescent light bulb to increase its lifetime and decrease operating temperature. The bulbs are rapidly replacing in-

candescent lamps, however they have lifetimes limited to less than 10,000 hours and generate as much as 150 degrees of heat.

The NXP technologist also outlined a range of new designs in existing silicon technology that could help reduce growth in greenhouse gas emissions. "The big win we can achieve is in power reduction in end equipment," he said.

For example, he described an improved TV backlight technology that if used in just ten percent of all sets could save 39 terawatt hours of energy per year. That's many times the 1.5 TWh/year NXP uses to make all its chips.

[Source: EETimes]

"Now the equation is different, and the industry has a role to play optimizing power use." said Rene Penning de Vries.

## NEWS

## IMEC joins the SOI Industry Consortium



The SOI Industry Consortium, aimed at accelerating

silicon-on-insulator (SOI) innovation into broad markets, announced today that IMEC has joined the organization as an academic member. IMEC is a world-leading independent nanoelectronics research center headquartered in Leuven, Belgium. It has been active in the field of SOI technologies for more that two decades.

"SOI has long been one of the key routes on IMEC's roadmaps. In semiconductor technology, platform creation is of vital importance in making progress, creating critical mass,

and identifying common interests between various players. That is what IMEC is doing, and that is what the SOI Industry Consortium is doing. We support the activities of the consortium and look forward to moving forward together," says Luc Van den hove, Chief Operating Officer and Executive Vice President of IMEC.

"We are extremely pleased to have IMEC as part of the SOI Consortium," says Horacio Mendez, Executive Director of the SOI Industry Consortium. "IMEC is recognized as one of the world's leading semiconductor R&D institutes. The expertise and knowledge they bring to this partnership will

be exceptionally valuable in maximizing SOI's capabilities."

IMEC's collaborative CMOS scaling research platform targets technology generations two to three nodes ahead of state-of-the-art IC production. The activities are organized as a cluster of programs enabling very advanced research. Based on its long-standing track record and expertise, IMEC's central focus in these programs is on advanced process module and device research including the exploration of new materials. Beside fundamental studies related to device physics, IMEC is also processing both partially depleted (PD) and fully depleted (FD) SOI devices.

[Source: SOI Industry Consortium]

IMEC is a world-leading independent nanoelectronics research center headquartered in Leuven, Belgium

## FEATURES

## Executive Outlook: Survival and Opportunities in 2009



**Martin van den Brink**  
Executive VP  
Marketing and Technology, ASML

Manufacturing chips with features of 32 nm and below brings about significant challenges that will force closer working synergies among all aspects of IC design and production — what we call "holistic manufacturing." In lithography, the immediate challenges will be in double patterning, but the same needs will hold true for extreme ultraviolet (EUV) in the future. In both cases, chipmakers will have to manage operations with smaller margins for error and higher stakes than ever before, and incremental adaptations will not provide acceptable levels of risk and reward.

Currently, design for manufacturing (DFM) is the mainstream approach to chip pro-

duction — incorporating many manufacturing techniques that are developed and implemented separately for each wafer processing area. For the lithographic process, this entails increasingly complex off-line adjustments to mask patterns and shapes before the designs are delivered to the fab. This approach has served well, but it is running out of steam — at 32 nm and below, margins for CD uniformity and overlay approach the atomic level. Therefore, the lithographic process must become more holistic and integrate all of the separate off-line disciplines, and it can no longer use a single generic model of one scanner.

A holistic approach must place more emphasis on pushing computational lithography to the fab floor in applying full-chip modeling and analysis to fleets of scanners. Metrology data will be used to further fine-tune the scanners. This is the only way to

achieve the needed precision under real-world conditions, and ensure reliable production ramp of future chip designs.

Execution of holistic lithography, of course, is a tremendous challenge — a computational lithography task of the highest order will need to be available to chipmakers. But once implemented, fleets of scanners can be quickly optimized for every layer of every design, and the worlds of design and manufacturing will have moved several large steps closer.

and the world around them. According to one forecast, for example, large-screen HDTV sales are expected to soar to 250 million units in 2013, compared with 65 million in 2007.

The semiconductor industry must be prepared to meet the device demand that will accompany such growth. Semiconductor suppliers must invest in new products, processes and services, and streamline their cost structures. Good companies will emerge from 2009 leaner and stronger. And which companies are "good"? Those with the scale, development resolve, organizational stability, and financial resources to exploit the downturn and thrive in the next recovery.

## Franklin Kalk

Executive Vice President and  
CTO, Toppan Photomasks



Semiconductor industry forecasts agree that 2009 will be a difficult year, with second-half improvement appearing unlikely. Layoffs, financial losses, plant closures and company restructurings have begun to dominate the news, and the challenges for photomask makers mirror the semiconductor industry's malaise.

Downturns have a way of accelerating industry restructuring and forcing difficult

decisions. While most visible in memory manufacturing, silicon foundries and EDA companies, the need for consolidation is also evident in mask manufacturing. Reduced trailing-edge demand, which is likely to be permanent, has led to plant closures and delayed investments. Programs to extend optical lithography as far as possible still are pursued, if only to avoid costly and risky technology migrations. But almost everything else is under critical review.

Though the timing is debatable, demand will return for new electronic products to connect consumers to the Internet, each other,

## ANNOUNCEMENT

## International Summer School on Advanced

## Microelectronics. MIGAS 2009



MIGAS Summer School is designed to foster and promote expertise in new, advanced topics of microelectronics. The aim of MIGAS is to offer every year a forum of detailed presentations on emerging topics of microelectronics.

It is also a unique opportunity for senior and junior researchers to update their knowledge in a very specific and emerging field. MIGAS brings together scientists from all over the world and from research institutes, universities, R&D small, medium and large com-

panies.

This year 2009 MIGAS Summer School will be held from 21st - 27th June in Autrans-Grenoble, a reknown resort, dedicated to alpine and cross-country skiing in winter, and to tourism in summer, located in the Regional Natural Park of the Vercors mountains, 30 km away from Grenoble.

MIGAS 2009 topic is "Advanced SOI concepts: from materials to devices and applications".

The lectures will be given by world-class experts, including: J-P. Colinge (Ireland), T.

Hiramoto (Tokyo), A. Zaslavsky (USA), R. Schrimpf (USA), C. Fenouillet-Béranger

(STMicroelectronics), A. Asenov (Glasgow), O. Faynot, T. Ernst and B. de Salvo (LETI), F. Gamiz (Granada), S.

Cristoloveanu (Grenoble), etc.

Details and information for registration will be soon available on the MIGAS website: <http://www.migas.inpg.fr/>



## FEATURE

## SOI Technology Goes Mainstream

Ruth DeJule

Semiconductor International

More than a decade ago, the first commercially available devices based on silicon-on-insulator (SOI) technology were introduced in IBM's high-end 0.25  $\mu\text{m}$  servers — the result of a 20-year journey from initial bonding of silicon-on-sapphire substrates. Today, SOI-based products (Fig. 1) can be found wherever speed, functionality and low power consumption are needed, including servers, processors, printers, game consoles, network and storage systems, and ultralow-power applications such as wristwatches and automotive applications. "We are seeing with each new technology generation the market opening up for SOI, driven by client interest and SOI's ability to solve unique problems," said Mark Ireland, vice president, semiconductor platforms at IBM (Essex Junction, Vt.).

To help facilitate market expansion, the SOI Industry Consortium (Austin, Texas) was formed in late 2007, and has 25 members from foundries, equipment manufacturers, IDMs and independent design houses. The objective to ease SOI's transition into the mainstream begins by putting in place the necessary infrastructure and ecosystems.

#### What makes SOI unique?

Where bulk technologies start with a single-crystal silicon substrate, the SOI starting material has an embedded oxide layer just below the silicon surface. The significance is a reduction in leakage current and power/performance advantages over devices designed and built in bulk wafers.

Internal studies at IBM comparing 45 nm SOI-based circuits to the same circuits in 45 nm bulk yield 30% performance benefit using transistors of comparable leakage. "If higher performance is not required for your design, the SOI advantage can be turned into a lower-power design point," Ireland said. As much as 40% lower power has been demonstrated. Further studies indicate lower soft

error rates are also intrinsic to SOI technology, with a 5–7 $\times$  improvement over bulk.

Furthermore, SOI-based devices generally have better temperature sensitivity so that they can be operated at high temperatures and latchup does not exist because device isolation prevents parasitic bipolar device formation between FETs.

Some advantages over bulk are also seen in processing, such as not requiring complex isolation techniques nor deep n and p channel implantations. As technologies scale, bulk processes must add extra processing steps to implantations and STI modules — overhead that SOI eliminates.

#### Two types of devices

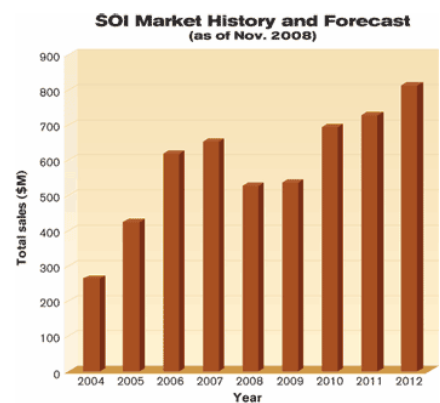
SOI devices can be fully depleted or partially depleted, where the amount of depletion refers to the channel region of a transistor. Partially depleted SOI transistors resemble their bulk counterparts, where doping concentrations in the channel determine the depletion depth, leaving a neutral silicon "floating body" isolated from the grounded substrate residing below the buried oxide.

In contrast, a thin-film SOI transistor in which the depletion region extends down to the buried oxide, leaving no neutral region, is considered fully depleted. Fully depleted transistors require an ultrathin silicon film to control short-channel effects, where the threshold voltage ( $V_t$ ) depends heavily on the gate length, and in general provide only low- $V_t$  transistors.

#### Looking ahead

SOI technology can potentially provide the platform for other materials beyond SOI. For example, it could incorporate high-mobility materials such as GaAs and InP, which are extremely expensive and cannot be used as full wafers. Alternatively, they may be placed either on top of SOI or, using the technology, placed locally on the surface to form islands of high-mobility substrates.

Other types of layers have been considered such as putting strained silicon on an insulator to increase device performance by introducing strain into the transistor channel. However, in one demonstration, the remaining strain proved too little to enhance performance in the final transistor product. Strain was introduced more effectively through modifications made during wafer processing. Similarly, IMEC used a substrate with strain upon which to build finFETs, but the strain relaxed completely as fin sizes approached 20 nm, Jurczak said, resulting in only a small performance benefit of 5–10%.



1. The graph indicates a steady increase in revenue after 2009, with the total market reaching ~\$800M by 2012. (Source: VLSI Research Inc.)

There is no doubt SOI is an attractive choice for key markets, giving its strong position in the industry. Though the demand for SOI products declined in 2008, this was a reflection of a macroeconomic trend in the semiconductor market in general, according to VLSI Research's Zlatan Kremonic. However, he said, "Stable growth is seen after 2009 (Fig. 1), with the total market reaching ~\$800M by 2012, indicating a 22% increase over last year's earnings."

As wafer prices come down and processes are fine-tuned, other consumer markets that push performance with the lowest possible active power — such as digital television and high-end mobile Internet device space — will necessarily opt for SOI-based devices.



## EUROSIO Network

**Thematic network on silicon on insulator technology, devices and circuits.**

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: [eurosoi@ugr.es](mailto:eurosoi@ugr.es)

The EUROSIO network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSIO aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

# CALENDAR

**- 215th ECS Meeting**

San Francisco, California.

May 24th - 29th, 2009

**- 13th International Workshop on Computational Electronics IWCE 2009**

Beijing, China

May 27th - 29th, 2009

**- MIGAS International Summer School**

Autrans-Grenoble, France.

June 20th - 26th, 2009

**- INFOS 2009**

Clare College, Cambridge, United Kingdom.

June 29th - July 1st, 2009

**- European School On Nanosciences & Nanotechnologies**

Grenoble, France.

August 23rd - September 12th, 2009

**- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference**

Athens, Greece.

September 15th - 19th, 2009