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## HIGHLIGHT NEWS

## Smart power semiconductor technology reduces po-

### wer consumption



**STMicroelectronics** claims the next

**generation variation of its smart power technology could enable significant reductions in the power consumption of a range of electronic systems.**

The company has produced a demonstrator chip with a medical equipment supplier for ultrasound scanners. Current technology typically handles eight channels, but according to ST the new semiconductor technology can handle more than 100 channels. Potential applications include new medical equipment and battery chargers in hybrid electric vehicles.

The new technology is a variation of

ST's Bipolar cmos-dmos (BCD) smart power semiconductor technology that combines silicon on insulator (SOI) substrate technology with 0.16 $\mu$  lithography. According to ST, this will enable chip designers to combine high density logic circuitry (1.8 and 3.3V cmos) with full dielectric isolation and a component portfolio including power mosfet transistors that can operate up to 300V, low noise devices, and high value resistors, leading to asics that cannot be implemented using conventional bulk silicon substrates.

"Semiconductor technologies that can drastically reduce electrical energy consumption in consumer and industrial appliances have existed in the labs for many years and their potential contribution to the

reduction of worldwide power consumption is significant," said Claudio Diazzi, group vice president, Technology R&D, STMicroelectronics. "However, the cost of these technologies has previously been too high to make them commercially viable. We believe that this new smart power technology will make a significant difference." The development of the technology is part of an advanced European R&D project.

[Source: New Electronics]

## CONFERENCE

### FD SOI Workshop in Taiwan



The SOI Industry Consortium, CEA-Leti and Soitec organized the 5th edition of the FDSOI Workshop at the Ambassador Hotel, in Hsinchu, Taiwan on April 28 following the VLSI-TSA and VLSI-DAT conferences (April 25-27, 2011).

This workshop was co-organized by Dr. H. Mendez from the SOI Industry Consortium, Dr. O. Faynot from CEA-Leti and Dr. C. Mazure and

Mrs. B.-Y. Nguyen from Soitec.

As the industry is preparing for the 14nm node that many believe will require a fully depleted device architecture, planar FDSOI offers today an excellent value proposition with an evolutionary CMOS solution for 20nm for low power and high speed. Published data show VT variability reduction by 60%, and best Ion/Ioff ratios from VDD IV down to 0.5V compared to bulk based processes. FDSOI technology enables low VDD operation for logic and high-density SRAM cells at sub-0.6V

VDD regime with excellent SNM and minimum cell size. Using an ARM Cortex™-M0 core, a team of SOI Industry Consortium members demonstrated that planar FDSOI technology enables designers to continue to decrease the voltage to reduce the overall power, while maintaining system performance.

More information:

[Http://www.soiconsortium.org](http://www.soiconsortium.org)

FEATURE

# The SOI Papers at ISSCC 2011

“the SOI papers were also notable for work reducing power consumption, extending scalability and overcoming threshold voltage variation”, says Hars



**Adele HARS**  
Advanced Substrate News

The International Solid-State Circuits Conference – better known as ISSCC – is of course where the big guns show us their big advances at the chip level. At the most recent conference, held a few weeks ago in San Francisco, advances that leveraged SOI were once again at the forefront.

As always, performance gains generate plenty of buzz. But the SOI papers were also notable for work reducing power consumption, extending scalability and overcoming threshold voltage variation.

IBM presented the world’s highest frequency microprocessor to date, clocking in at 5.2 GHz. On 45nm SOI, it’s the first commercial processor ever to break through the 5GHz speed barrier, and is the centerpiece of Big Blue’s new zEnterprise 196 system.

In another paper, IBM presented the first embedded high-k/metal-gate (HK/MG) SRAM on 32nm SOI enabling operation at down to 0.7V.

AMD presented its Bulldozer 2-core modules, which are on 32nm SOI with HK/MG. Clocking in at 3.5GHz, we’ll see them beginning in desktop and server Fusion chips this year.

In a quieter but clearly significant paper, ST and Leti compared 65nm low power (LP) partially depleted (PD) SOI with standard 65nm LP CMOS bulk. They found that PD-SOI, when combined with a low resistivity produced with forward body bias of the power switch, can reduce leakage current by 52.4% vs. bulk and increase the frequency by 20% at 1.2V, while decreasing power by 30% at 360MHz.

For summaries of additional SOI-based papers at ISSCC and other recent conferences, see ASN’s PaperLinks.

[Source: Advanced Substrate News]

NEWS

## Soitec announces major U.S. CPV

### solar power project



**Soitec** Ventures Selects Soitec’s Concentrix

CPV Solar Power Technology To Produce 150 Megawatts of Clean Energy For San Diego Gas & Electric

Soitec will build a new 200MW CPV manufacturing facility in the San Diego region.

[Source: SOITEC]

REMEMBER:

**2011 International SOI Conference deadline for contributions is May 16th**

CONFERENCE

## 2011 SOI Conference. Deadline for submission



Submission period for 2011 International SOI Conference is **May 16th, 2011**.

For over 35 years the IEEE International SOI Conference has been the premier meeting of engineers and scientists dedicated to current trends in Silicon-on-Insulator technology. Sponsored by the IEEE Electron Devices Society, the conference traditiona-

lly provides a forum for open discussion in all areas of SOI technologies and applications as well as the introduction of new developments presented in original papers presented at the technical sessions.

More information as well as a detailed programme can be found at the conference site:

<http://www.soiconference.org>



Tempe Mission Palms Hotel and Conference Center

FEATURE

# SOI for MEMS: A Promising Material



**Éric MOUNIER**  
Yole Développement

Although MEMS technologies are not driven by CD shrinking as ICs, that does not mean MEMS do not undergo strong technological evolutions. The ever-growing MEMS markets, today mostly driven by consumer applications, now have to be performance-driven, cost-driven and size driven.

SOI wafers are a promising substrate for MEMS manufacturing. We estimate the SOI market for MEMS devices will be close to \$100M by 2015 (see Figure 1). That represents a CAGR (2011-2015) of 15.6% for SOI, compared to 8.1% for bulk silicon-based solutions.

One main reason for using SOI is to have more design freedom. Tronics, for example is using SOI with High Aspect Ratio Micromachining technology. This technology was developed to manufacture high performance custom inertial sensors (accelerometers and gyroscopes).

Other reasons cited for choosing an SOI-based solution for MEMS include the need for the smallest possible package, very tight control and precision of the structure, ability to withstand high pressure and temperature, long product lifetime, smallest possible die size and reduced cost.



Substrate Market for MEMS

Additional features in SOI wafers can further simplify MEMS design and manufacturing. For example, “cavity-SOI”, in which the SOI wafer has pre-etched cavities, enables the MEMS manufacturers to focus on their core competencies in reducing development time, which in turn can even lower production costs. Some MEMS manufacturers have found that pre-etched SOI cavities combined with dry etching simplifies the release of the devices.

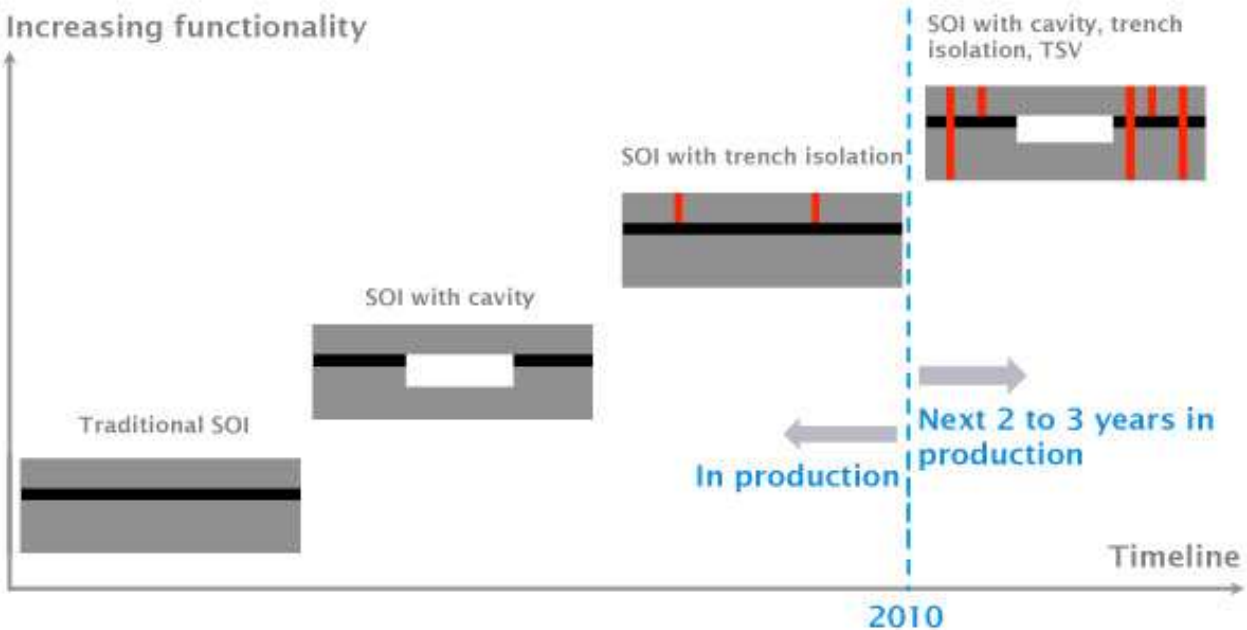
MEMS manufacturers using cavity-SOI include VTI Technologies, Invensense and other players in the seismic accelerometer (Tronics) and pressure sensor markets.

Figure 2 shows a roadmap for SOI wafers for MEMS. From “traditional” SOI, we are now using SOI with pre-etched cavities. Further developments will allow the realization of SOI wafers with trench isolation, cavities and Through Silicon Vias (TSV).

Suppliers of other substrate solutions are following similar added-value paths. Glass, for example, can be used as a thin wafer carrier for wafer level capping and/or packaging with Through Glass Vias interconnect.

Overall, we believe substrates will provide additional functionalities in the future, enabling more integrated MEMS devices.

[Source: Advanced Substrate News]



Roadmap for SOI wafers for MEMS



## EUROSIO Network

**Thematic network on silicon on insulator technology, devices and circuits.**

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: [eurosoi@ugr.es](mailto:eurosoi@ugr.es)

The EUROSIO network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSIO aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

# CALENDAR

**- ULIS 2011**

Cork (Ireland)  
March 14th-16th, 2011

**- ESSDERC ESSCRIC 2011**

Helsinki, Finland  
September 12th-16th, 2011

**- FD SOI Workshop**

Hsinchu (Taiwan)  
April 28th, 2011

**- 2011 IEEE International SOI Conference**

Tempe, Arizona (USA)  
October 3rd-6th, 2011

**- 219 ECS Meeting**

Montreal (Canada)  
May 1st-6th, 2011

**- 220 ECS Meeting**

Boston, MA (USA)  
October 9th-14th, 2011

**- International Symposium on Circuits and Systems. ISCAS 2011**

Rio de Janeiro, Brazil  
May 15th-18th, 2011

**- 221 ECS Meeting**

Seattle, Washington (USA)  
May 6th-11th, 2012