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## EDITORIAL

### EUROSUI+: The balance of the first year.



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The main and last objective of EUROSUI Network is to establish Europe as the international scientific leader in Silicon on Insulator (SOI) Technology, Devices, Circuits and Systems. In this sense, the EURO-SUI+ co-ordination efforts during this first year have been focused on the starting of those activities which contribute to improving the role of the European Semiconductor Industry with regard to SOI and to the knowledge that will enable Europe to compete internationally. Although EUROSUI achievements during FP6 have been many and very important for the European SOI technology, and the situation of SOI technology in Europe has greatly improved during the last three years, there are plenty of challenges at the near future. Even if we now are in the right direction, Europe is still far away from the pursued international leadership. After the elaboration of the State-of-the-Art report and EURO-SUI Roadmap, we have identified the main actors, the strong points and weaknesses of Silicon-On-Insulator technology in Europe. All this information is collected in the EUROSUI Roadmap, where the challenges which will have to be faced in the future are also identified. Our first stage was a passive one (collecting and structuring the information). This second stage is being much more active; we are not only looking at around us, collecting and re-structuring the available information,

but we have passed to the action in a more active role, developing the tasks, fostering creation of consortiums and leading the projects and proposals which give Europe and the European Semiconductor Industry the international leadership which they deserve as pioneers and big developers of SOI technology.

The best way to reach this goal is to try to spread the SOI technology all over Europe, making it accessible to any European semiconductor actor:

*"We want that SOI technology is reachable to any European research group or Fabless Semiconductor company; we want that any circuit design has the chance to become a SOI circuit using European technology."*

To do so, we have to work in three directions:

- Training of researchers and engineers in the particularities of this technology, i.e., in the design of circuits taking advantage of SOI technology.

- Spreading and promotion of the benefits and advantages of SOI technology.

- Development of a platform which offers SOI technology for the actual fabrication of SOI circuits

It is widely accepted by the International Semiconductor Community that most of the electronic circuits (in the whole application spectra) will have a better performance, and therefore, they will be more competitive, if they are built using SOI technology. However, nowadays it is not easy to have access to this technology, even when we count in Europe with some of the most advanced SOI technologies all over the World.

Up to now, a lot of research activities have been pursued in Europe around SOI at different levels: substrate, device, and circuit.

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## ANNOUNCEMENT

### Tutorial Section on

### the EUROSUI Website Complete



Following the efforts that the EUROSUI team is making to improve its work and with the dedication that has been shown thus far, the new tutorial section is now complete containing the different tutorials held since the first EUROSUI Works-

hop in Granada in 2005.

The different tutorials are organized according to their dates and places and a search engine by years has been also developed. For further details take a look at:

<http://www.eurosui.org/tutorials.asp>

## EUROSOI+ BALANCE

## EUROSOI+ activities

## during the first year

The following two points summarize EUROSOI+ activities during this period:

I. **Training and promotional activities.**

a) **Website database**

<http://www.eurosoi.org>

i. **EUROSOI Virtual Journal**

<http://www.eurosoi.org/articles.asp>

ii. **EUROSOI Landmark publications**

[http://www.eurosoi.org/landmark\\_publications.asp](http://www.eurosoi.org/landmark_publications.asp)

iii. **EUROSOI Newsletters**

<http://www.eurosoi.org/newsletters.asp>

iv. **EUROSOI News&Announcements**

<http://www.eurosoi.org/news.asp>

v. **EUROSOI Training material database**

<http://www.eurosoi.org/tutorials.asp>

b) **Organization of Training events and Tutorials**

i) Multigate SOI MOSFETs (January 23<sup>rd</sup>, 2008, Cork, Ireland, 2008)

ii) SOI from modelling to design (January 19<sup>th</sup>, 2009, Goteborg, Sweden)

c) **Organization of Workshops.**

i) **Fourth Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits**

(Tyndall National Institute, Cork, Ireland, Jan 23-25<sup>th</sup>, 2008):

<http://www.tyndall.ie/eurosoi2008/>

(56 communications, 80 attendants)

ii) **Fifth Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits**

(Chalmers University of Technology, Goteborg, Sweden, Jan 19-21<sup>st</sup>, 2009):

<http://chalmers2009.eurosoi.org>

(60 communications, 90 attendants)

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**EUROSOI+: The balance of the first year. (cont.)**

Since few years, advanced SOI technologies have been developed in research labs in order to address the downscaling required for 32nm nodes and below. Today such researches are mainly dedicated to technology development. Among the various ones, we can mention the LETI Fully Depleted SOI technology (developed with high-k and metal gate) that currently has enough maturity to be evaluated at circuit level. So, it becomes obvious that a research-dedicated platform is necessary in order to address the circuit design aspects, focussing on the advantages of such technology for Low Power applications. Access to such platform is a long-time wish of European researchers. Hence, the main goal of EUROSOI+ is to coordinate the formation of such research-dedicated platform which will provide, through the integration in EUROPRAC-TICE, prototyping and Multi-Project-Wafers (MPW) in SOI open to all European companies using LETI SOI process in two-three years. We are co-ordinating all the activities which will make this platform a reality in 2010.

“Although EUROSOI achievements during FP6 have been many and very important [...], there are plenty of challenges at the near future.” said Francisco Gámiz.

“We want that SOI technology is reachable to any European research group or Fabless Semiconductor company; we want that any circuit design has the chance to become a SOI circuit using European technology.”

## EUROSÔI+ BALANCE

## EUROSÔI+ activities during the first year (cont.)

## d) Discussion Panels. The opinion of SOI experts.

- i) “Key Issues in SOI: Solutions and Ideas”, chaired by Prof. Sorin Cristoloveanu, January 24<sup>th</sup>, 2008, Cork, Ireland

Participants:

Dr. Damien Bretegnier, SOITEC  
 Prof. Denis Flandre, UCL  
 Dr. Segei Okonin, Innovative Silicon  
 Dr. Olivier Faynot, CEA-LETI  
 Prof. Jean-Pierre Colinge, Tyndall

- ii) “What is the killing advantage of multiple-gate SOI MOSFETs: electrostatics and scalability, transport or functionality”, chaired by Prof. Sorin Cristoloveanu, January, 20<sup>th</sup>, 2009 Goteborg, Sweden

Participants:

Prof. Cor Claeys, IMEC  
 Prof. Jerry Fossum, University of Florida  
 Prof. Jean-Pierre Colinge, Tyndall  
 Dr. Olivier Faynot, CEA-LETI  
 Dr. Stephane Monfray, STMicroelectronics, Crolle  
 Prof. Francis Balestra, IMEP, SINANO Institute

## e) Student and travel grants.

- 13 student grants to attend EUROSÔI workshops have been given to PhD students who works towards their PhD in European Universities in the field of SOI technology.
- 20 travel grants have been also distributed among EUROSÔI network partners to partially cover their registration and travel expenses to attend EUROSÔI workshops.
- Financial support for major conferences and promotional travels.

## f) Scientific Exchanges

- 7 Exchange visits of EUROSÔI members to other European Research Centers have been funded by EUROSÔI+ during this first year.

## g) Elaboration &amp; Upgrading of Technical Focused Reports (TFRs).

- i) EUROSÔI State of the art report:  
[http://www.eurosoi.org/public/EUROSÔI\\_State\\_of\\_the\\_art.pdf](http://www.eurosoi.org/public/EUROSÔI_State_of_the_art.pdf)

- ii) EUROSÔI roadmap.  
[http://www.eurosoi.org/public/EUROSÔI\\_Roadmap.pdf](http://www.eurosoi.org/public/EUROSÔI_Roadmap.pdf)

- iii) EUROSÔI who is who.  
[http://www.eurosoi.org/public/EUROSÔI\\_who\\_is\\_who.pdf](http://www.eurosoi.org/public/EUROSÔI_who_is_who.pdf)

- iv) Benchmark of UTB vs. FinFET vs. DG SOI transistors. Which SOI device is favourite and for which application?  
[http://www.eurosoi.org/public/D4.15.focused.report.utb\\_finfet\\_def.pdf](http://www.eurosoi.org/public/D4.15.focused.report.utb_finfet_def.pdf)

II. Development of EUROSÔI fabrication & prototyping platform for the design of low-power SOI circuits.

- a) **Coordination of information exchange on LETI FDSOI technology.** FDSOI wafers with functional devices have been provided to UCL, and IMEP. Also, electrical measurements have been provided to UGR. On November 17th-18th, Dr. Olivier Faynot from LETI organized in Grenoble a tutorial (free of charge for the EUROSÔI members) focused on the training of European scientists on Fully Depleted SOI technology. Well recognized technologists, as well as international experts on devices and circuit design trained the attendees on SOI specific aspects, including: (1) Devices physics; (2) Technology description; (3) Modelling and circuit design; (4) Variability issues; (5) FDSOI platform development status. See the link: <http://www.eurosoi.org/tutorialinfo.asp?id=7>

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## EUROSOI+ BALANCE

## EUROSOI+ activities during the first year

(cont.)

“The main goal of EUROSOI+ is to coordinate the formation of a research-dedicated platform” says Francisco Gámiz.

**b) Coordination of activities for the documentation, promotion and spreading of Research-dedicated Design Kit (RDKit).** The development of the research design kit is progressing in phase with what has been planned in the European project called DECISIF. This design kit contains a digital part that includes device model, Design Rules Control file and Layout Versus Schematic file. These files are essential to model and control the layout generated by the designers. This part is completed at 85%. The design kit contains also an analog part that includes Matching parameters, RF parasitics and related model (completed at 50%). The design kit finally contains an automated digital Design flow that includes Standard cell library and SRAM memory cuts. This last part is completed at 30%. With such level of achievement, the design kit can already be used to design some elementary circuits. It is scheduled to complete this design kit by mid-2009.

**c) Promotion of the FDSOI technology.** Promotion of the FDSOI technology has been made by LETI during this period to

the following companies:

- Presentation of the technology and results are regularly (every 3 months) made to SOITEC.
- Technology and electrical results have been also presented to ST Microelectronics in order to highlight the interest of such technology for Low Power applications.
- Promotion of FDSOI technology has also been done to AMD and ARM through a presentation at the SOI consortium meeting in November 2008. More detailed meetings will be planned for each company in 2009

**d) Coordination of activities for the evaluation of the possible integration by the end of 2009 in the existing EURO PRACTICE structure.**

We are now considered as one of the EURO PRACTICE projects (<http://www.europpractice.org/>).

We participated in the EURO PRACTICE Workshop held in Leuven on September 4<sup>th</sup>, 2008.

## ANNOUNCEMENT

## International Summer School on Advanced Microelectronics. MIGAS 2009



MIGAS Summer School is designed to foster and promote expertise in new, advanced topics of microelectronics. The aim of MIGAS is to offer every year a forum of detailed presentations on emerging topics of microelectronics.

It is also a unique opportunity for senior and junior researchers to update their knowledge in a very specific and emerging field. MIGAS brings together scientists from all over the world and from

research institutes, universities, R&D small, medium and large companies.

This year 2009 MIGAS Summer School will be held from 21<sup>st</sup> - 27<sup>th</sup> June in Autrans-Grenoble, a renowned resort, dedicated to alpine and cross-country skiing in winter, and to tourism in summer, located in the Regional Natural Park of the Vercors mountains, 30 km away from Grenoble.

MIGAS 2009 topic is “Advanced SOI concepts: from materials to devices and applications”.

The lectures will be given by world-class experts, including: J-P. Colinge

(Ireland), T. Hiramoto (Tokyo), A. Zaslavsky (USA), R. Schrimpf (USA), C. Fenouillet-Béranger

(STMicroelectronics), A. Asenov (Glasgow), O. Faynot, T. Ernst and B. de Salvo (LETI), F. Gamiz (Granada), S. Cristoloveanu (Grenoble), etc.

Details and information for registration will be soon available on the MIGAS website: <http://www.migas.inpg.fr/>





## EUROSIO Network

**Thematic network on silicon on insulator technology, devices and circuits.**

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: [eurosoi@ugr.es](mailto:eurosoi@ugr.es)

The EUROSIO network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSIO aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

## CALENDAR

**- 215th ECS Meeting**

San Francisco, California.

May 24th - 29th, 2009

**- 13th International Workshop on Computational Electronics IWCE 2009**

Beijing, China

May 27th - 29th, 2009

**- MIGAS International Summer School**

Autrans-Grenoble, France.

June 20th - 26th, 2009

**- INFOS 2009**

Clare College, Cambridge, United Kingdom.

June 29th - July 1st, 2009

**- European School On Nanosciences & Nanotechnologies**

Grenoble, France.

August 23rd - September 12th, 2009

**- 39th European Solid State Device Research Conference and 35th European Solid State Circuits Conference**

Athens, Greece.

September 15th - 19th, 2009

**- 2009 IEEE International SOI Conference**

Foster City, California.

October 5th - 8th, 2009