THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

# EUROSOI Newsletter

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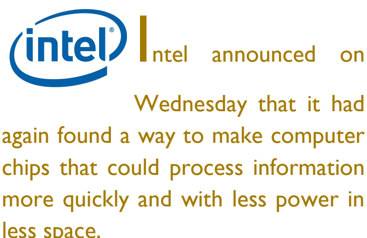
## HIGHLIGHT NEWS Intel Increases Transistor Speed by Building Upward



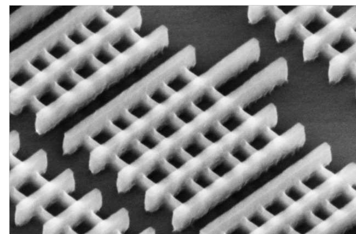
Intel announced on Wednesday that it had again found a way to make computer chips that could process information more quickly and with less power in less space.

The transistors on computer chips — whether for PC's or smartphones — have been designed in essentially the same way since 1959 when Robert Noyce, Intel's co-founder, and Jack Kilby of Texas Instruments independently invented the first integrated circuits that became the basic building block of electronic devices in the information age.

These early transistors were built on a flat surface. But like a real estate developer building skyscrapers to get more rentable space from a plot of land, Intel is now building up. When the space between the billions of tiny electronic switches on the flat surface of a computer chip is measured in the width of just dozens of atoms, designers needed the third dimension to find more room.

The company has already begun making its microprocessors using a new 3-D transistor design, called a Finfet (for fin field-effect transistor), which is based around a remarkably small pillar, or fin, of silicon that rises above the surface of the chip. Intel, based in Santa Clara, Calif., plans to enter general production based on the new technology some time later this year.

Although the company did not give technical details about its new process in its Wednesday announcement, it said that it expected to be able to make chips that run as much as 37 percent faster in low-voltage applications and it would be able to cut power consumption as much as 50 percent.



Intels's new transistors have tiny pillars, or fins that rise above the chips's surface

Intel currently uses a photolithographic process to make a chip, in which the smallest feature on the chip is just 32 nanometers, a level of microscopic manufacture that was reached in 2009. (By comparison a human red blood cell is 7,500 nanometers in width and a strand of DNA is 2.5 nanometers.) "Intel is on track for 22-nanometer manufacturing later this year," said Mark T. Bohr, an Intel senior fellow and the scientist who has overseen the effort to develop the next generation of smaller transistors.

The company's engineers said that they now felt confident that they would be able to solve the challenges of making chips through at least the 10-nanometer generation, which is likely to happen in 2015.

The timing of the announcement Wednesday is significant, Dr. Bohr said, because it is evidence that the world's largest chip maker is not slipping from the pace of doubling the number of transistors that can be etched onto a sliver of silicon every two years, a phenomenon known as Moore's Law. Although not a law of physics, the 1965 observation by Intel's co-founder, Gordon Moore, has defined the speed of innovation for much of the world's economy. It has also set the computing industry apart from other types of manufacturing because it has continued to improve at an accelerating rate, offering greater computing power and lower cost at regular intervals.

However, despite its promise and the company's bold claims, Intel's 3-D transistor is still a controversial technology within the chip industry. Indeed, a number of the company's competitors say they believe that Intel is taking a what could be a disastrous multibillion-dollar gamble on an unproved technology.

There has been industry speculation that Finfet technology will give Intel a clear speed advantage, but possibly less control over power consumption than alternative approaches.

By opting for a technology that emphasizes speed over low power, Intel faces the possibility that it could win the technology battle and yet lose the more important battle in the marketplace. The scope of Intel's gamble is underscored by the fact that while the company dominates in the markets for data center computers, desktops and laptops, it has largely been locked out of the tablet and smartphone markets, which are growing far more quickly than the traditional PC industry.

Those devices use ultra-low-powered chips to conserve battery power and reduce overheating.

[*Continues on page 2*]

## NEWS Intel Increases Transistor Speed by Building Upward (*cont*)

*But like a real estate developer building skyscrapers to get more rentable space from a plot of land, Intel is now building up..*

Apple, for example, uses Intel's microprocessors for its desktops and laptops, but for the iPhone and iPad it has chosen to use a rival low-power design, built by others, that Apple originally helped pioneer in the late 1980s.

Industry executives and analysts have said that Intel is likely to have a lead of a full generation over its rivals in the shift to 3-D transistors. For example, T.S.M.C., the Taiwan-based chip maker, has said that it does not plan to deploy Finfet transistor technology for another two years.

Other companies, like ST Microelectronics, are wagering that an alternative technology based on placing a remarkably thin insulating layer below traditional transistors will chart a safer course toward the next generation of chip manufacturing. They believe that the insulation approach will excel in low-power applications, and that could be a crucial advantage in consumer-oriented markets where a vast majority of popular products are both hand-held and battery-powered.

"Silicon-on-insulator could be a win in terms of power efficiency," said David Lammers, the editor in chief of Semiconductor Manufacturing and Design Community, a Web site. "From what I am hearing from the S.O.I. camp, there is a consensus and concession that Finfets are faster. That's the way you want to go for leading-edge performance."

In a factory tour here last week, Intel used a scanning electronic microscope to display a computer chip made using the new 22-nanometer manufacturing process. Viewed at a magnification of more than 100,000 times, the silicon fins are clearly visible as a series of walls projected above a flat surface.

It is possible to make transistors out of one or a number of the tiny fins to build switches that have different characteristics, such as faster switching speeds or extremely low power. Looking at the chip under less magnification, it is possible to see the wiring design, which appears much like a street map displaying millions of intersections.

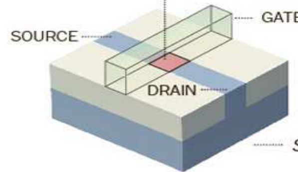
Despite the impressive display, Intel's executives acknowledge the challenge the company is facing in trying to catch up in the new consumer markets that so far have eluded it.

"The ecosystem right now is not aligned in our favor," said Andy D. Bryant, Intel's chief administrative officer, who now runs the company's technology and manufacturing group. "It has to be good enough for the ecosystem to take notice and say, 'We better pay attention to those guys.' "

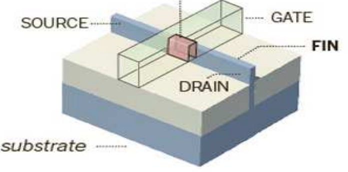
**New Transistor Grows in the Third Dimension**

The new Intel transistor provides higher performance by increasing the conductive area between the source and drain regions of the chip, allowing more current to flow through.

**TRADITIONAL TRANSISTOR**
Planar **conductive area**



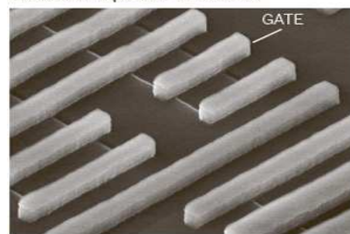

**NEW INTEL TRANSISTOR**
Conductive area is expanded on **three sides of a raised fin**



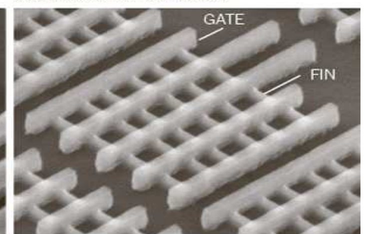

*Silicon substrate*

The new transistor with its raised **fin** requires a smaller footprint, allowing more of them to fit in a computer chip. The new design can also reduce power consumption, yielding better battery life on devices.

Traditional planar transistor




Intel Tri-Gate transistor




Source: Intel THE NEW YORK TIMES

## CONFERENCE 2011 SOI Conference. Deadline for submission

Submission period for 2011 International SOI Conference **has been extended till May 30th, 2011**.

For over 35 years the IEEE International SOI Conference has been the premier meeting of engineers and scientists dedicated to current trends in Silicon-on-Insulator technology. Sponsored by the IEEE Electron Devices Society,the conference traditionally provides a forum for open discussion in all areas of SOI technologies and applications as well as the introduction of new developments presented in original papers presented at the technical sessions.

FEATURE

# GPU/CPU on SOI: the Xbox 360 did it first

**Microsoft and IBM moved the CPU and the GPU of the best-selling game console in North America onto a single SoC – a year ahead of the pack.**

There's a lot of excitement about the "latest trend" of integrating both the computing chip – the CPU and the graphics chip – the GPU – into a single chip. But in fact, the first GPU/CPU system-on-chip (SoC) came out in June 2010. It's on 45nm SOI, is produced by multiple foundries, and is at the heart of the hottest selling game console in North America: the Xbox 360.

The technical community refers to it as the Xbox 360 S – "S" for "slim", because the new chip enabled a host of slimming effects. The two most important were a slimmed-down power budget (43% less than the previous generation) and a serious reduction in the bill-of-materials (always good news for the bottom line).

**Power down**

You might think that the GPU/CPU combo also provided a major performance boost. But in fact, for game console lifetimes, one thing you can't do is toy much with performance. Game developers count on having a stable platform – they need it to work just the way they first planned it for the entire console life cycle.

One of the advantages SOI gives to chip designers is that it's a powerful "knob to turn" – they can ratchet up performance (and keep about the same some power budget), or drastically reduce power (in exchange for a less dramatic performance increase), or they can find a balance somewhere in between.

In the case of the Xbox 360 GPU/CPU, one can surmise that since they couldn't boost performance too much, they had the luxury of turning the knob way down for power. And that translates into a whole lot of benefits.

But first let's look at what they actually did.

**2 for 1**

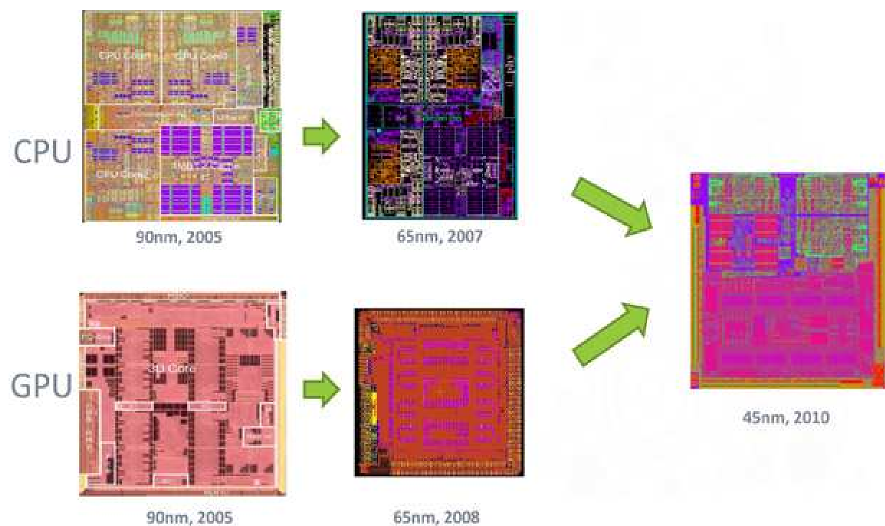
The first Xbox 360 came out in 2005, with a CPU on 90nm SOI (see ASN #6) and a GPU on 90nm bulk. A few years later, the chips were migrated to 65nm. Then in 2010, the two were combined on a single chip using 45nm SOI.

For the IBM and Microsoft chip design team, the latest challenge involved both a port (the bulk GPU to SOI), a shrink (to 45nm) and a complete redesign of the GPU (which had originally been designed by ATI). However, from a graphics standpoint, the resulting chip had to remain functionally identical to the old GPU, to ensure the backward compatibility of the games.

It also involved removing the front-side bus (FSB), which handles functional intercommunication between the CPU and GPU blocks.

Compared to having two chips, putting the two units into one chip saved 60% in power and 50% in area compared to the 90nm versions.

[*Source: Advanced Substrate News*]




FEATURE

# ESD Protection for Advanced SOI

Shuqing (Victor) CAO
**GlobalFoundries**

Technology scaling unfavorably affects the electrostatic discharge (ESD) protection of integrated circuits mainly by reducing MOSFET oxide and junction breakdown voltage, diode current shunting capability, and by increasing the interconnect resistivity. The I/O data-rate increasingly limits the capacitive budget, exacerbating the shrinkage of ESD design space.

It is important to find ESD solutions that minimize parasitic loading while achieving superior robustness.

Silicon-on-insulator (SOI) technology presents some distinctive challenges to ESD design. The buried oxide (BOX) layer makes vertical and deep body ESD structures infeasible. The lateral SOI diode based ("rail-based") protection approach is becoming less effective in the high-current Charged Device Model (CDM) domain, owing to excessive voltage build-up along the ESD path involving power buses, power-clamps (Pclamp), and diodes.

The pad-based "local clamping" scheme is a promising option. By connecting an ESD device directly between the pad and Vss, it allows the ESD current to flow from the pad to ground without going through the resistive path (shown as crossed out in Figure 1) and the Pclamp. This way, the pad voltage is considerably reduced, immediately expanding the design space.

[*Source: Advanced Substrate News*]

EUROSOI Network

**Thematic network on silicon on insulator technology, devices and circuits.**

**The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EURO-SOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.**

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

# CALENDAR

**- 219 ECS Meeting**
Montreal (Canada)
May 1st-6th, 2011

**- International Symposium on Circuits and Systems. ISCAS 2011**
Rio de Janeiro, Brazil
May 15th-18th, 2011

**- ESSDERC ESSCRIC 2011**
Helsinki, Finland
September 12th-16th, 2011

**- 2011 IEEE International SOI Conference**
Tempe, Arizona (USA)
October 3rd-6th, 2011

**- 220 ECS Meeting**
Boston, MA (USA)
October 9th-14th, 2011

**- 221 ECS Meeting**
Seattle, Washington (USA)
May 6th-11th, 2012