THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

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HIGHLIGHT NEWS

IBM Announces Highest Performance Embedded Processor for System-on-Chip Designs

IBM Corporation announced the industry's highest performance, highest throughput processor for system-on-chip (SoC) product families in the communication, storage, consumer, and aerospace and defense markets.

LSI Corporation has collaborated with IBM on the development of the processor core, called the PowerPC® 476FP. LSI intends to utilize the 476FP PowerPC core in its next-generation multicore platform architecture for networking applications.

The PowerPC 476FP operates at clock speeds in excess of 1.6 GHz, and 2.5 Dhrystone MIPS (million instructions per second) per MHz, delivering over two times the performance of IBM's most advanced embedded core currently available for the original equipment manufacturing (OEM) market. This level of performance also positions the 476FP as the highest performing embedded processor for System-on-Chip designs yet announced and available in the industry.

The processor extends the scalability of IBM's Power Architecture® in traditional embedded applications, and provides a growth platform for emerging applications such as 4G networks and WiMax infrastructure products.

The processor dissipates just 1.6 watts at these performance levels when fabricated in IBM's 45-nanometer, silicon-on-insulator (SOI) technology, positioning the 476FP as one of the most energy efficient embedded processor cores in the industry.

The 476FP offering includes an architectural extension of IBM's CoreConnect local bus technology (PLB6), supporting coherency for multiple processors and providing a level of scalability that is ideal for customers designing families of products and focusing on software re-use. The 476FP provides a seamless performance boost to all customers currently using the PowerPC 4xx family of processor cores, maintaining IBM's long-standing practice of protecting legacy software investments.

"We are pleased to announce this new embedded PowerPC processor," said Richard Busch, IBM director of ASIC products. "This high-performance, power efficient, compact processor core allows customers to meet the needs of today's applications, while preserving legacy code. Our collaboration with LSI brings together IBM's expertise in processor development with LSI's experience in networking and storage architectures, optimizing this core to address today's high-speed embedded requirements."

LSI has designed a configurable level 2 (L2) memory cache that is tightly coupled to the processor, which helps the PPC476 achieve its leading performance. There are three configurations of the L2 (256K, 512K and 1M) to allow customer optimization in a given application.

"LSI will be the first to offer products with the PowerPC 476FP core produced from our close collaboration with IBM," said Gene Scuteri, vice president, Networking Components Division, LSI. "Our use of the PowerPC 476 core, along with the configurable L2 cache that LSI developed as part of the collaboration, results in a powerful multicore processor subsystem that is well suited to future networking applications. The PowerPC 476 is a key building block in the next-generation multicore platform architecture from LSI."

[*Source: IBM*]

ANNOUNCEMENT

First Call for the Sixth EUROSOI Workshop

First announcement and opening of online abstract submission for the EUROSOI 2010 Workshop to be held from 25th-27th January 2010 in Granoble (France) have just been launched.

More information on page 2

FEATURE

Building an SOI IP/EDA Infrastructure

As with all new technologies, SOI brings about a chicken-and-egg kind of situation. IP availability is needed to drive adoption, but most third-party IP providers will want to see adoption before moving ahead

Richard Goering

My last blog on silicon-on-insulator looked at the low-power benefits of SOI. But performance and power gains are meaningless if you can't design and manufacture a chip. Fortunately, the needed infrastructure to support SOI design is falling into place.

As the SOI Consortium noted in a Design Automation Conference presentation, the SOI semiconductor ecosystem is expanding. Foundry support is available from Chartered, GlobalFoundries, Freescale, IBM, and UMC. SOI-ready libraries and silicon IP, memory IP, EDA tools and methodologies, and design services are all available from various providers. As the presentation notes, one tool that supports SOI implementation is the Cadence Encounter Digital Implementation System.

ARM, which has been a strong supporter of SOI, offers a physical IP SOI library portfolio. It includes a standard cell library, I/O library, memories, and tools. At the recent Design Automation Conference, Cadence announced validation of 45 nm IBM SOI ASIC libraries from ARM using the Encounter Digital Implementation System. "This should accelerate the IP infrastructure build-out," commented Jeff Wolf, director of membership development at the SOI Consortium.

According to Rahul Deokar, product marketing director at Cadence, SOI does not significantly change the IC design flow. The main challenge for EDA tools is to correctly model the "history effect" that occurs because the threshold voltage of a transistor may depend on its previous states. This occurs because of the "floating body" transistor effect.

Chin-Chi Teng, vice president of research and development at Cadence, added that Cadence accurately accounts for the history effect in library characterization and that these models are then seamlessly used during timing/signal integrity (SI) analysis and design optimization. He said that Cadence offers a "two-pass" signal-integrity analysis capability that's especially useful for SOI. It mostly operates at the cell level, but has the capability to drop down to the transistor level for critical portions of the chip to ensure that no SI violation is missed.

"The Cadence SOI design flow is very pushbutton," Rahul said. "You just bring in the characterized library, and all of the other steps are the same IC design flow."

The biggest enabler for SOI, Rahul said, will be the availability of libraries and IP. "I believe the libraries are getting ready," he said. "IP will be an ongoing process." While there is "increasing interest for sure" in SOI, he noted, adoption is so far mainly limited to the IBM ecosystem.

As with all new technologies, SOI brings about a chicken-and-egg kind of situation. IP availability is needed to drive adoption, but most third-party IP providers will want to see adoption before moving ahead. I think ARM deserves a lot of credit for jumping in ahead of the curve. Now it's up to SOI advocates to make a strong enough case for the technology to move it from specialized, high-performance applications into the IC design mainstream.

[*Source: Cadence*]

NEWS

First Call for the EUROSOI 2010 Workshop

IMPORTANT:

Online Abstract Submission now available for the EUROSOI 2010 Workshop

EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008) and Göteborg (2009), EUROSOI 2010 will be held in Grenoble, France. It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and application-oriented engineers.

Abstract submission is now available online at the Workshop website **http://chalmers2010.eurosoi.org** as well as complementary information.

NEWS

ARM 1176 in IBM SoI process demonstrates a cell-based flow

For several years it has been clear that SoI processes have a more favorable speed vs. voltage characteristic than comparable-node bulk silicon processes. This advantage can mean either lower operating voltage at a given speed---and thus lower power—or higher performance at a given voltage. And the presence of vast quantities of both the Xbox 360 and the PlayStation-3 should eliminate any question about volume manufacture, at least from IBM. So why is SoI still so rarely used?

The normal answer is the lack of design infrastructure. Early on, most SoI designs were at the high-performance fringe, and so people rightly associated SoI with custom design and highly-skilled teams. It would require new device models, new libraries, and new tools to make SoI work in a normal cell-based RTL flow, this reasoning said.

But three papers at the IEEE International SoI Conference strongly suggest that the situation has changed. Jean-Luc Pelloie of ARM, Kevin Kranen of Synopsys, and Michael Jacobs of Cadence described implementation of a synthesizable ARM 1176 core with its associated memories and I/Os in IBMs 45nm SoI CMOS, using an off-the-shelf Synopsys-based standard flow. Pelloie's paper described the design decisions and results, while Kranen's and Jacobs's papers described the flow and how it was possible to use standard tools.

[*Source: EDN*]

ANNOUNCEMENT

6th International SemOI Conference and 1st Ukrainian-French Seminar

First announcement and call for papers for the 6th International SemOI Conference and 1st Ukrainian-French Seminar to be held from 26th-30th April 2010 in Kyiv (Ukraine) have just been launched.

The goal of the Conference is to debate about the recent developments in nanometer down scaled Semiconductor-on-Insulator (SemOI) Systems which are basis blocks for modern high-sensitive sensors in a wide range of applications such as telecommunications, radiation control,, boimedical instrumentation, Chemicals análisis, etc.

Download announcement in pdf format at *http://www.eurosoi.org*

NEWS

Leti's Planar-SOI Technology Meets Low-Power, 22nm Node Requirements, Supports Development of "Green" Products

Leti, a leading global research center committed to creating and commercializing innovation in micro- and nanotechnologies, today presented results at the SOI Industry Consortium workshop in Leuven, Belgium, that prove SOI-based planar CMOS meets requirements for low-power, 22nm node devices, offering a practical route to further feature shrink and enabling a significant jump for "green" products.

With unmatched access resistance and electrostatic characteristics, planar SOI is superior to other technologies based on bulk CMOS technology and FinFET architecture. It also shows outstanding performances for low-power applications requiring 22nm technology, such as consumer electronic devices including 4G mobile phones.

"Many transistor architectures have been proposed for the 22nm node and below. At Leti, we favored planar technologies for faster and easier transition to manufacturing," said Laurent Malier, CEO of Leti. "Our recent results prove the strength of this approach. Together with the recent ARM results demonstrating power reduction on 45nm technology, we have proven that SOI technologies offer solutions for low power at a wide variety of nodes, including 22nm and below. Furthermore, we have demonstrated that planar SOI dramatically improves the energy performances of many products that will change our lives, while offering long-term success for many companies involved in these fast-growing markets."

In addition, drain-induced barrier lowering (DIBL) below 100mV/V has been demonstrated and SOI has been proven to enable the reduction of electrostatic parasitics.

While variability is a major challenge to be addressed for the 22nm node, Leti's results prove that variability control is possible with today's state-of-the-art SOI wafers. In particular, variability on threshold voltage was reduced by a factor of two compared with FinFET technologies, at wafer and batch levels.

Leti also showed that fully depleted SOI (FDSOI) CMOS can be scaled down to the 10nm node through tuning the buried oxide and silicon layer thickness. Displayed results show that FDSOI approach also addresses the variability issues for this further shrink.

CEA is a French Research and Technology Organization, with activities in three main areas: Energy, Technologies for Information and Healthcare, and Defence and Security. Within CEA, the Laboratory for Electronics & Information Technology (CEA-Leti) works with companies in order to increase their competitiveness through technological innovation and transfers. Leti is focused on micro and nanotechnologies and their applications, from wireless devices and systems, to biology and healthcare or photonics. Nanoelectronics and Microsystems (MEMS) are at the core of its silicon activities. As a major player in the MINATEC innovation campus, LETI operates 8,000-m² state-of-the-art clean rooms, on 24/7 mode, on 200mm and 300mm wafer standards.

[*Source: NanoTechWire*]

EVENTS

ISCAS 2010

The IEEE International Symposium on Circuits and Systems (ISCAS) is the world's premier networking forum of leading researchers in the highly active fields of theory, design and implementation of circuits and systems.

ISCAS 2010, sponsored by the IEEE Circuits and Systems Society and supported by the Institut Supérieur d'Electronique de Paris, will be held in Paris, France from 30 May to 2 June 2010.

The Symposium will focus on circuits and systems employing nanodevices (both extremely scaled CMOS and non-CMOS devices) and circuit fabrics (mixture of standard CMOS and evolving nano-structure elements) and their implementation cost, switching speed, energy efficiency, and reliability.

NEWS

SOI Industry Consortium announces SOI Design Clinic at ARM TechCon3

The SOI Industry Consortium today announced an initiative to deliver a silicon on insulator (SOI) educational event in conjunction with ARM TechCon3 to help the electronics industry reap the benefits of SOI. Responding to the industry's need for education in this area, the SOI Design Clinic will provide IC designers and engineering management with a technical understanding of significant differences between designing on SOI versus bulk silicon, and how to receive the power-saving, integration, reliability and performance advantages of SOI. Respected experts from the semiconductor industry will deliver training and share their insights at this practical and timely event, to help attendees evaluate and plan their move to SOI.

Shrinking semiconductor feature sizes demonstrate that CMOS on bulk silicon is rapidly reaching its technological limits for many applications. Process complexity, variability, short-channel effects, leakage, power density, and reliability are just a few reasons why technology leaders transition to SOI. Today available foundry processes, libraries, EDA tools and designer training are making SOI accessible to fabless semiconductor companies and OEMs, and enabling first-time SOI design teams to achieve improved power, performance and area results in their customary design cycle times, as documented by ARM in a recent study.

The design clinic will take place in the Santa Clara Convention Center (California) on October 21, 2009, co-located with ARM TechCon3

[*Source: SOI Industry Consortium*]

NEWS

ARM teaches world how to use SOI process technology

ARM is working with the SOI Industry Consortium to run a silicon on insulator (SOI) design seminar.

The company recognises a need to help IC designers understand the significant differences between designing on SOI versus bulk silicon, to achieve power-saving and integration benefits.

The mantra coming out of this event is that srinking semiconductor feature sizes demonstrate that CMOS on bulk silicon is rapidly reaching its technological limits for many applications.

There is a theory that ARM could force a rethink on low-power process technology

ARM is claiming potential power savings of up to 40% using a silicon-on-insulator (SOI) 45nm test chip.

The SOI process, an alternative to the traditional bulk CMOS process used to fab ARM-based processors, was demonstrated on a test chip was based on an ARM 1176 processor.

According to ARM, the demonstration shows that SOI technology is a "viable alternative to traditional bulk process technology when designing low-power processors".

"Process complexity, variability, short-channel effects, leakage, power density, and reliabilityre just a few reasons why technology leaders transition to SOI," said the SOI Industry Consortium.

Foundry processes, libraries, EDA tools and designer training are making SOI accessible to fabless semiconductor companies.

[*Source: ElectronicsWeekly*]

IMPORTANT:

December 1st is the deadline for Abstract Submission fot the EUROSOI 2010 Workshop

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EUROSOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- NanoICT School 2009
San Sebastián, Spain.
October 26th - 30th, 2009

- EUROSOI 2010 Workshop
Grenoble, France.
January 25th - 27th, 2010

- 217 ECS Meeting
Vancouver, Canada.
April 25th - 30th, 2010

- International Symposium on Circuits and Systems. ISCAS 2010
Paris, France.
May 30th - 2nd, 2010

- ESSDERC ESSCRIC 2010
Sevilla, Spain.
September 13th - 17th, 2010

- 218 ECS Meeting
Las Vegas, USA.
October 10th - 15th, 2010