THEMATIC NETWORK ON SILICON ON INSULATOR TECHNOLOGY, DEVICES AND CIRCUITS.

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HIGHLIGHT NEWS CEA-Leti makes a R&D 20nm Fully Depleted SOI process available through CMP

CEA-Leti and CMP (Circuits Multi Projets®) announced during the FDSOI Workshop at Tokyo University the launch of an Exploratory MPW (Multi Project Wafers) initiative based on FDSOI (Fully Depleted SOI) 20nm process, opening the access of its 300mm infrastructure to the design community. This MPW offer is partly supported by EUROSOI+ network that gathers the main European academic partners on SOI.

"The Leti has pioneered the SOI technology for years, leading track records in the most advanced research in FDSOI, assessing its key advantages for low power high performance applications with several industrial customers" said Laurent Malier, CEO of the CEA-Leti. "It is time now to enlarge the diffusion of the FDSOI technology enabling test case on 20nm process and beyond. This hit will change the game, breaking the wall of technology to give an open access to the R&D international design community and a unique opportunity to touch Silicon with innovative designs."

"CMP is very proud to offer such a very advanced process to the community. Such a process will allow Researchers and Engineers to experiment the benefits of SOI on an advanced technology node" said Bernard Courtois, head of CMP.

CEA-Leti has been involved with FDSOI R&D for a number of years and has developed internally both an advanced High-K/Metal Gate FDSOI process and a number of specific design and simulation tools based on industry standard design flow packages. FDSOI technology presents key advantages over conventional bulk technology for future nodes. The electrostatic integrity of the transistors is ensured by the thinness of the body without the need for extra litho steps, like in the case of FinFETs, or of channel doping. The consequence is a planar technology that exhibits at the same time excellent short channel behaviour and significant improvement of the variability as shown in a number of recent papers.

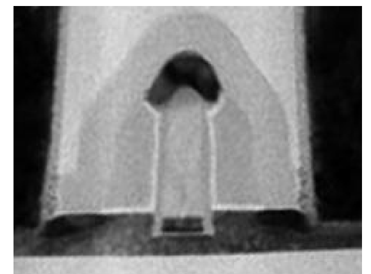
The basis of our technology offer will be the following:

•CMOS transistors with an undoped channel and a silicon film thickness of 6nm

•High-k / Metal Gate stack

•Single threshold voltage (Vth) n- and pMOSFET with balanced Vth of ±0.4V

•Associated Design Kit, including SPICE model (Verilog-A language), model cards extracted from silicon data, p-cells, DRC, LVS, schematic, parasitics



•Design Kit documentation

The first run is scheduled to be launched in September 2011. All details will be available on the CMP website.

[*Source: CEA-Leti*]

ANNOUNCEMENT Registration opened for EUROSOI 2011

Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be held at Granada, Andalucía (Spain) **from January 17th to January 19th.** It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

Registration form is now available online at the Workshop web site. Early registration is possible before January 4th. Participants are also allowed to attend only to the Training course or to the Conference.

Special prices are offered for students.

All the information at:

http://granada2011.eurosoi.org

NEWS

Soitec announces global alliance with Johnson Controls to capture utility scale solar energy projects

The combination of the respective strengths of both companies [...] will provide an unbeatable force to accelerate and widen the successful installation of solar renewable energy utility scale plants.

Soitec, the world's leading supplier of silicon-on-insulator (SOI) and advanced solutions for the electronics and energy industries, announced that its Concentrix Solar division focusing on concentrator photovoltaic (CPV) systems, has concluded a global alliance with Johnson Controls (NYSE: JCI), the global leader in delivering products, services and solutions that increase energy efficiency in buildings.

Johnson Controls provides turnkey project development, engineering, procurement, construction, operation and maintenance of large scale energy efficiency and renewable energy projects. Under this collaboration, Johnson Controls and Concentrix Solar will identify and respond to commercial opportunities for the project development, and construction of utility scale solar energy facilities. Johnson Controls will build, operate, maintain and provide lifecycle support for solar installations using Concentrix CPV technology.

The combination of the respective strengths of both companies: efficient and cost effective technology on the one hand, and a worldwide leader in energy efficiency and sustainability on the other hand, will provide an unbeatable force to accelerate and widen the successful installation of solar renewable energy utility scale plants in Direct Normal Irradiation (DNI) regions across the globe.

"Before forming our alliance with Concentrix Solar, we studied all primary solar technologies and market participants. We concluded that the combination of Soitec's technical capabilities in engineered substrate solutions and Concentrix Solar's module design together provides the market leading solution for solar power generation in high DNI regions around the world," stated Iain Campbell VP & GM of Global Energy and Workplace Solutions, Johnson Controls.

"We are delighted to team up with Johnson Controls, who shares our vision for sustainable and economically viable, solar renewable energy," said André-Jacques Auberton-Hervé, chairman and CEO, Soitec. "Together, we understand the market opportunity and positive environmental impact that solar renewable energy power will bring to both existing and future facilities, and are excited to provide integrated solutions to our customers."

Concentrix Solar's cost effective and innovative CPV technology, with its high efficiencies and two-axis tracking, is ideally suited to areas in the world that have high direct solar irradiation.

Concentrix Solar will exhibit in booth #2701 at Solar Power International, October 12-14 in Los Angeles.

FEATURE

Planar fully depleted SOI: the technological solution against variability

F. Andrieu, O. Weber, J. Mazurier, O. Faynot
CEA-Leti

[FDSOI architecture] improves the variability of the electrical characteristics thanks to an undoped channel.

It is well known that the planar fully depleted silicon-on-insulator (SOI) (FDSOI) architecture is a technological booster of the CMOS performance, thanks to better electrostatics than devices on bulk. This article shows that it also greatly improves the variability of the electrical characteristics, thanks to an undoped channel. This leads to good matching performance.

This technology mainly addresses low-power applications, even if it is compatible with wafer-level or process-induced stressors for high performance. In particular, it yields a 22% energy-consumption reduction at a given speed for ring oscillators at the 45nm node compared to the same circuit on bulk. Finally, one of the main advantages of this technology is the low variability obtained.

The variability issue and solution

For the 20nm CMOS technology node and below, the variability of the electrical characteristics is becoming as important as the electrical performances themselves. Especially, the threshold-voltage (VT) variability is a key for the stability of the SRAMs, which represent a huge proportion of an integrated circuit area. Indeed, improving the VT variability directly lowers the SRAM dispersions and, in turn, the minimal supply voltage (VDDmin) of the memory blocks.

Historically, for CMOS on bulk, the dopant concentration in the

[*continues on page 4*]

NEWS

Training Course Programme and Key-Note talks of EUROSOI 2011

As in previous editions of EUROSOI Workshop, this international event covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and applications oriented engineers.

Typical topics include:

(1) Synthesis of advanced SOI wafers (Ge, SiGe and strained layers, SOI heterostructures)

(2) Materials evaluation, properties of ultra-thin films and buried oxides, defects and stress, interface quality

(3) SOI MOSFETs: characterization, modeling and simulation of typical mechanisms, parameter extraction, reliability issues

(4) Circuit design, process and applications: low power/voltage and RF circuits, innovative memories, high voltage devices, imagers, sensors, photovoltaics and MEMS

(5) More than Moore perspectives: multiple-gates, 3D stacks of devices and circuits, nanowires, NEMS, tunneling transistors, heterogeneous integration etc.

For 2011 edition to be held next January in Granada (Spain)., EUROSOI is trying its best and now putting the final touches.

Although there are still some details missing that will be announced soon, the final programme for the Training Course, Key-Note Talks and Workshop has been scheduled and is now available:

Monday, January 17th. Training Course. Tutorial.

- 9.15h-9.30h: Introduction and Tutorial Overview. *F. Gámiz (University of Granada)*
- 9.30h-10.30h: SOI solutions for next technological nodes. *Prof. Sigfried Mantl, FZJülich, Germany*
- 10.30h-11.30h: ETSOI Technology. *Dr. Bruce Doris, IBM, USA*
- 12.00h-13.00h: CMOS-SOI-MEMS Imagers. *Prof. Y. Nemirovsky, Technion, Israel*
- 15.00h-16.00h: SOI Low-power applications. *Dr. N. Sugii, LEAP, Japan*
- 16.00h-17.00h: Memories on SOI. *TBD*
- 17.30h-18.30h: SOI Photonics. *Dr. Jean Marc Fedeli, LETI, France*
- 20.00h-21.30h: Welcome Reception at Hotel Nazaries

Tuesday-Wednesday, January 18-19th. Workshop

Key-Note Talks.

- FDSOI Ecosystem. *Dr. Carlos Mazure, SOITEC, France*
- Monte Carlo transport of advanced SOI devices. How far can we go? *Prof. Max Fischetti, UTDallas, USA*
- Nanoelectronics: the point of view of EU Commission *TBD*

NEWS

Student Grants for EUROSOI 2011

To foster the participation of students to the Training Course and to EUROSOI 2011 Workshop, **EUROSOI will give 15 grants to Ph.D. students** which submit and defend a contribution to EUROSOI workshop.

The grant will consist on **the waiver of the registration fee (tutorial and Workshop) and the accommodation** (4 nights of hotel at Hotel Luna, Granada) from Sunday, January 16th to Thursday, January 20th, 2011. If you are a Ph.D student you can apply for these student grants when you submit your contribution.

EUROSOI 2011. IMPORTANT DATES:

- **Dec. 1st, 2010: Deadline for abstract submission.**
- **Dec. 15th, 2010: Notification of acceptance.**
- **Dec. 31st, 2010: Deadline for advanced registration.**

ANNOUNCEMENT

Abstract Submission for EUROSOI 2011

The submission period for EUROSOI 2011 is now open until December 1st.

In this edition an extended abstract must be submitted online through the Workshop web site

http://granada2011.eurosoi.org

using the available abstract template.

Abstracts exceeding the 2 pages limit will be rejected.

Following the Workshop, the committee will select the best contributions and offer their authors the opportunity to submit an extended version to Solid-State Electronics.

Students are strongly encouraged to send their contributions in order to be eligible for one of the appealing grants offered in this edition by the organization.

Authors will be notified of acceptance in mid-December

Detail of the Alhambra and the Palace of the Emperor Carlos V

FEATURE Planar fully depleted SOI: the technological solution against variability (cont.)

Variability performance is much better for planar FDSOI than for planar bulk technology, for which variability is governed by random dopant fluctuation within the channel, and much than for FinFETs, for which the fin width fluctuation is the limiting parameter.

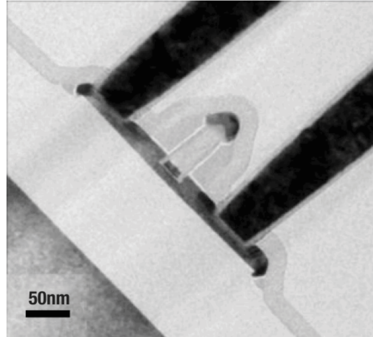


Fig.1. TEM image of a transistor on FDSOI with a Tbox=145nm thick Buried Oxide (BOX), L=30nm gate length and a mesa isolation.

channel of the transistors (Ndop) increases node after node (by a factor k) when the device dimensions (the active width W, the gate length L and the effective gate oxide thickness in the inversion regime Tinv) are scaled by a factor 1/k. This scaling law is only based on electrostatic considerations and not on variability considerations. However, for sub-65nm CMOS, one of the most important showstoppers is the VT variability, which is no longer negligible. Actually, the VT standard deviation varies as

$$\sigma_{V_T N_{dop}} \propto T_{inv} \cdot \frac{\sqrt[4]{N_{dop}}}{\sqrt{W.L}}$$

when it is limited by the random dopant fluctuation (RDF). This means that the intrinsic variability of CMOS on bulk theoretically degrades node after node (by a factor $k^{1/4}$). For the moment, the solution used by IC manufacturers to keep the VT standard deviation of the nominal device quite constant with the scaling is not to play on the channel doping but to slow down the (gate length L and supply voltage Vdd) scaling or to counterbalance by electrostatic improvements (Tinv lowering or junction optimizations) or by design solutions. However, for the 20nm node and below, considerations on the dynamic power consumption require a Vdd scaling and electrostatic/performance considerations already require a challenging Tinv.

In this context, we propose another paradigm based on the planar FDSOI with undoped channels. In this architecture, the scaling is not governed by the channel doping but rather by the film thickness below the gate (Tsi). This enables an excellent electrostatic behavior (better than CMOS on bulk) without any intentional channel doping. Such devices thus resist the root cause

$$\sigma_{V_T,L} \propto \sigma_L \cdot \left(\frac{dV_T}{dL}\right)_{T_{inv},T_{Si},V_d}$$

of the RDF (i.e., the channel doping) and simultaneously improve the electrostatics. Indeed, FDSOI is really an electrostatic booster, similar to the Tinv reduction. This enables a lower sensibility of the VT vs. the gate length (L) and, consequently, an additional reduction of the second major source of variability in bulk devices, namely line edge roughness (LER). This latter indeed influences the VT standard deviation following:

(σL being the effective channel-length fluctuation). Finally, the two major sources of variability (RDF and LER) are strongly or even completely reduced thanks to the FDSOI architecture. This is evidenced by Fig. 2, which shows that the LER-induced fluctuation (in blue and red) can be neglected compared to the "surface" sources of variability attributed to the gate stack (charge or gate work-function fluctuations), even down to L=25nm.

Variability performance of FDSOI devices

Thanks to the undoped channel, we highlight a low variability, as evidenced by Fig. 3. It exceeds the one obtained on bulk devices or on

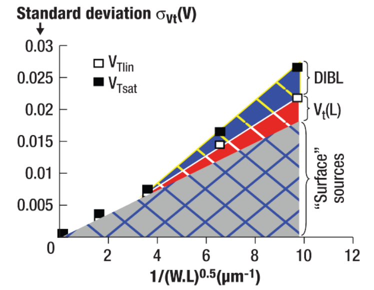


Fig. 2.Pelgrom plot with VT measured in the linear and in the saturation regime for TSi=8nm.

FinFETs (not shown here). Indeed, for 3D devices and, contrarily, as for planar FDSOI architectures, VT strongly depends on W. Thus, there is an additional contribution induced by the fluctuation of the fin width (Wfin), which is the smallest dimension of FinFETs:

$$\sigma_{V_T,W} \propto \sigma_{W_{fin}} \cdot \left(\frac{dV_T}{dW_{fin}}\right)_{T_{inv},T_{Si},V_d}$$

For planar FDSOI, however, SOI thickness (TSi) is the smallest dimension. However, Tsi is not defined by the lithography but rather by the Smart Cut process. This guarantees a very good process uniformity of Tsi. We demonstrated that the Tsi uniformity now reached by SOI wafer manufacturers (Tsi range around 10Å) is in the specifications for the 20nm node.

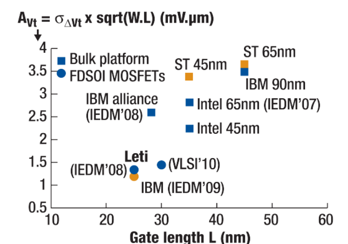


Fig.3. Benchmark of the matching factor vs. the gate length for bulk or FDSOI devices

[*Source: Solid State Technology*]

EUROSOI Network

Thematic network on silicon on insulator technology, devices and circuits.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). EURO-SOI aims at federating the existing research work on SOI topics and at providing an appropriate communication channel between academic groups and industrial production centres.

If you want to contribute to the EUROSOI Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

CALENDAR

- 2010 IEEE International SOI Conference
San Diego, California (USA)
October 11th-14th, 2010

- 218 ECS Meeting
Las Vegas, USA.
October 10th - 15th, 2010

- EUROSOI 2011 Workshop
Granada, Spain.
January, 17th-19th, 2011

- CDE 2011
Palma de Mallorca, Spain
February 8th-11th, 2011

- Ultimate Integration on Silicon Conference (ULIS)
Cork, Ireland
March 14th-16th, 2011

- 219 ECS Meeting
Montreal (Canada)
May 1st-6th, 2011