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HIGHLIGHT NEWS

IBM claims fastest MPU

 IBM Corp. said Wednesday (Sept. 1) that it will begin shipping Sept. 10 a new mainframe computer computer capable of 50 billion instructions per second, powered by 96 microprocessors with clock speeds up to 5.2 gigahertz.

IBM (Armonk, N.Y.) said the z196 processor is a four-core chip that contains 1.4 billion transistors on a 512-square millimeter surface. The chip was designed by IBM engineers in Poughkeepsie, N.Y., and was manufactured using IBM's 45-nm silicon-on-insulator process at the company's 300-mm fab in East Fishkill, N.Y., IBM said.

The mainframe processor makes use of IBM's embedded DRAM technology, which allows IBM to place dense DRAM caches, or components, on the same chips as high-speed microprocessors, resulting in improved performance, according to the company.

A spokesperson for IBM said the company was not disclosing any other z196 benchmark data at this time.

The new mainframe, the zEnterprise System, is the most powerful commercial IBM system ever, according to the company, capable of executing roughly 17,000 times more instructions per second than the most advanced system available in 1970, according to the company.

The z196 processor features new software to optimize performance of data-heavy workloads, including up to a 60 percent improvement in data intensive and Java workloads, according to IBM.

Last week, IBM engineers at the Hot Chips conference sketched out plans for a petaflops-class supercomputer built from as many as 64,000 Power7 processors.

The zEnterprise System offers 60 percent more capacity than its predecessor, the System z10, but uses about the same amount of electricity, IBM said. Energy efficiencies were achieved through

advances in microprocessor design, 45-nm silicon technology, more efficient power conversion and distribution and advanced sensors and cooling control firmware that monitors and makes adjustments based on environmental factors such as temperature and humidity levels and air density, according to IBM.

[Source: EETimes]

Soitec announces Concentrix Solar joining the Transgreen Initiative



Soitec the world's leading supplier of silicon-on-insulator (SOI) and advanced solutions for the electronics and energy industries, announced that its Concentrix Solar division focusing on concentrator photovoltaic (CPV) systems, has joined the Transgreen Initiative. Transgreen was recently created within the context of the Mediterranean Solar Plan to stimulate the development of a Trans-Mediterranean electric power transmission network to respond to the significant expected needs for electricity exchange between the two sides of the Mediterranean. Concentrix Solar's CPV technology is designed for use by large-scale solar power plants in hot and arid regions. The systems are extremely efficient, modular, flexible and very well-suited to the needs and challenges of the

Mediterranean region to produce low cost electricity.

"Transgreen is a perfect vector to support our activities in the Mediterranean area. We are looking forward to working with this ecosystem of companies and the countries of the Mediterranean region to demonstrate the value of CPV," said Concentrix Solar CEO, Hansjörg Lerchenmüller. "We have an opportunity to make a significant contribution to the region's energy needs for renewable energy sources and to export energy to European countries."

With 25 percent AC system efficiency, Concentrix Solar's CPV systems provide the highest efficiency of all solar technologies available. Especially at locations with extremely hot ambient temperatures, CPV systems perform better than conventional solar systems and therefore guarantee a high and constant power production throughout the day.

[Source: Soitec]

Anatomy Of A (Better) Gaming Platform

The original design was on 90nm and then migrated to 65nm [...] The size and power reduction possible with a 45nm process changed that architecture.

At the 45nm node and on an SOI process the design can be implemented with a method to minimize leakage and standby current.

Microsoft

Microsoft's third-generation Xbox360 engine uses a 45nm silicon on insulator (SOI) process—and a new architecture.

The original design was on 90nm and then migrated to 65nm. In both of these cases the fundamental architecture of the system remained the same—a CPU (central processing unit) chip, a GPU (graphics processing unit) chip, and memory management chip for the front-side bus (FSB) to the DRAM.

The size and power reduction possible with a 45nm process changed that architecture. With the ability to now integrate 347 million transistors on a single die, the new design is a single-chip CPU, GPU and FSB memory controller. The design features three CPU cores with L1 and L2 cache, a GPU core with GDDR3 memory interface, a video-out controller, a PCIe interface and a FSB manager. The chip is placed as part of a CPU module that includes a HSIO (high-speed input/output) interface to an EDRAM die.

Filling out the system is a South Bridge block that contains an interface to the system Flash, HDD, Optical Disk Drive, USB, IR Remote, and wireless 802.11n circuits. This architecture was chosen partly on the needs of the system and partly on the capability of the process. At the 45nm node and on an SOI process the design can be implemented with a method to minimize leakage and standby current. That allows Microsoft to bring these simultaneous high-power blocks onto a single monolithic die. The architecture includes system-level temperature sensors and control, as well as block-based power down. Using

the capabilities of the SOI, the power down is implemented with multiple power domains.

The chip now has 6 PLLs that support a total of 12 clock domains. The design uses an adaptive power supply system (APS), which results in 8 power domains. These separate the memory, CPUs and GPUs into different power domains, as well as the I/Os and interface logic. In order to facilitate interconnection to these blocks, the design used C4 pads on a 35mm PC-PBGA with a 3-2-3 buildup of layers. This reconfiguration resulted in a total net power reduction of more than 60% from the original design and more than 50% reduction in silicon area.

As the major blocks of the SoC came from different sources, the final chip was built using three different design methodologies. The CPUs were built using a semi-custom design methodology that supported synthesizable macros, full-custom macros, an 18-track, high-performance base library, a full independent clock grid and transistor-level timing analysis. The GPU area was built using an ASIC-style standard cell methodology—using a 12-track high-density (as opposed to high performance) base library, only synthesized macros, a combination of traditional H-Tree and full clock grid, and then finalized with

gate level timing analysis.

The overall chip and the block infrastructure were built using a full-chip hierarchical methodology that called the CPUs and GPUs as “hard macros” in the top level of the design. The timing was performed hierarchically and partitioned along the blocks and paths. The hierarchical nature required a mix of device-level and gate-level verification of the signals based on their criticality. At this top level, the chip design for test was put in and pushed down hierarchically through the blocks including the hard macros for the CPUs and GPU.

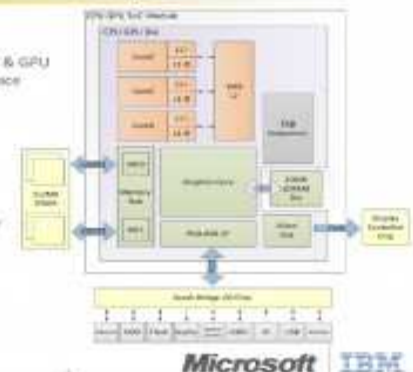
The top-level logic verification had a challenge from the new architecture: It had to be backward-compatible to support the existing library of games and have no change in game play. As a result, the design used sequential equivalence to validate the design. This is comparing the corresponding sequential path outputs from the two different design representations and making sure they are the same in both performance and function.

The advanced process provides for loss of capabilities in a new SoC, but with dramatic changes in device architecture and the incorporation of multiple design flows and tools to complete the task.

[Source: System Level Design]

Xbox 360 250GB System

- CPU-GPU SoC Module
 - CPU GPU Die
 - High Performance CPU & GPU
 - GDDR3 Memory Interface
 - Video Output
 - PCIe
 - Embedded DRAM Die
 - Custom South Bridge
 - IO Connectivity
 - System Management
 - Custom Video Display Controller
 - Optical Disk Drive
 - Flash and IO Connectivity
 - 250GB HDD
 - Wireless 802.11n Integration
- XBOX 360



NEWS

STMicroelectronics Powers High-End Mobile Internet and Video

Experiences on AMOLED Displays

STMicroelectronics, a leader in power semiconductors, is powering the AMOLED and Super AMOLED displays that enable today's advanced handheld devices to deliver high-quality web and video experiences on the move, with a family of ICs consolidating all the display module's power requirements in a single chip.

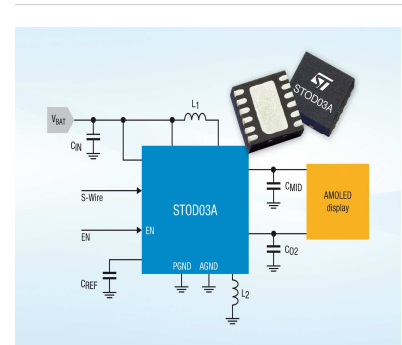
AMOLED (Active-Matrix Organic LED) technology enables sharp and vibrant images for mobile multimedia devices such as 3G smartphones and digital-still cameras. These devices do not use back-lighting and so offer key advantages over active-matrix LCDs, in terms of power saving and extremely low profile: typical thickness for AMOLED devices is now less than 1mm for the entire display module allowing stylish and space-efficient new designs. iSuppli has predicted annual shipments of phones with AMOLED displays will grow to more than 180 million

by 2014.

ST is the major provider of power-supply ICs for AMOLED displays. Its latest STOD03A provides the needed positive and negative supply voltages from a single chip, and improves on the performance of the well established STOD02. Only six external components are needed to complete the power-supply circuitry. Alternative approaches require more components and use more power, making ST's solution the most attractive for handset builders.

The STOD03A uses highly efficient synchronous operation for both voltage outputs, achieving up to 85% overall efficiency for longer overall battery life. Other power-saving features include automatic pulse-skipping operation for low power consumption at light loads, and a true shutdown mode drawing less than one microamp activated through the enable pin (EN). ST has achieved its high performance

using its Silicon-On-Insulator (SOI) technology as part of its latest-generation BCD fabrication process, which enables analog, digital and closely spaced high-power circuitry to be built on the same chip.



Compact, energy efficient AMOLED power chip increases battery life for super-slim 3G smartphones

IMPORTANT:

Abstract submission for EUROSOI 2011 will be opened soon.

ANNOUNCEMENT

Finalizing details for EUROSOI2011



EUROSOI Workshop is an international forum to promote interaction and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings in Granada (2005), Grenoble (2006), Leuven (2007), Cork (2008), Göteborg (2009) and Grenoble (2010), EUROSOI 2011 will be

held at Granada, Andalucía (Spain). It will include oral and poster sessions, outstanding keynote presentations, a training course, a social program as well as ample room for informal discussions.

Training course and Key-Note talks will be announced in the following Newsletter (October issue)

Detailed information:

<http://granada2011.eurosoi.org>

EVENT

ESSDERC / ESSCIRC 2010 in Sevilla

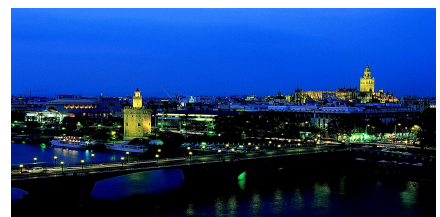


The 40th **European Solid-State Device Research Conference** (ESSDERC) and the 36th **European Solid-State Circuits Conference** (ESSCIRC) will be held in Sevilla this month (September 13th-17th)

The aim of the ESSDERC and the ESSCIRC conferences is to provide an annual European forum for the presentation and

discussion of recent advances in solid-state devices and circuits.

ESSDERC and its sister conference ESSCIRC are governed by a single Steering Committee. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts, and circuit and system designers.



Views of the Cathedral and the Torre del Oro

The 60-kW array consists of ten trackers and took about two weeks to install and commission.

NEWS

Safari lodge's concentrated photovoltaic plant could be precursor to 50-MW project

South Africa's first concentrated photovoltaic (CPV) solar demonstration plant of 60 kW was operational in the Western Cape, and supplying the daytime power requirements for the Aquila safari lodge, near Touws River.

The plant was built by German solar engineering company Concentrix solar, which is a subsidiary of France-based technology company Soitec.

Besides powering the game reserve,

the plant will become a training ground to develop solar skills in the area. Discussions are under way with the University of Cape Town's Energy Research Centre as to what kind of curriculum could be developed around the demonstration plant.

The 60-kW array consists of ten trackers and took about two weeks to install and commission. The

technical installation was done by Johnson Controls.

Each tracker consists of a number of concentrator modules comprising high-performance multijunction cells with a Fresnel lens, as well as an inverter and a tracking system.

[Source: Engineering News]

NEWS

Soitec strengthens industrial operations team with the nomination of Francis Taroni



Soitec, the world's leading supplier of silicon-on-insulator (SOI) and advanced solutions for the electronics and energy industries, announced today that the company has appointed Francis Taroni to the position of Senior Vice President, Industrial Operations. In keeping with the group's continuing growth and expanding operations, Taroni will develop and implement the most appropriate industrial organization for the development of Soitec, which is renowned for its strong high-volume production capabilities.

A graduate of the Ecole Française de Radioélectricité, d'Electronique et d'Informatique, Francis Taroni (52) has worked in the semiconductor industry for his entire professional career. He began in 1982 at IBM, where his responsibilities included various management roles in France and the United States. More recently, Francis Taroni has

NEWS

Soitec confirms Q2 2010-2011 outlook

Following recent news flow from the semiconductor industry, Soitec (Euronext Paris) confirmed today that it expects almost stable consolidated sales as compared to first quarter sales at constant exchange (i.e. 1.27). A slight decrease in total wafer sales around two percent at constant exchange should be offset by other Group activities including

Concentrix deliveries related to Chevron contract. Guidance for sequential total Group sales growth in H1 of around 20% is therefore confirmed.

Q2 sales for 2010-2011 will be published on 18th October 2010 after the close of the Paris Stock Exchange.

[Source: Soitec]

successively held posts as Chief Technology Officer and Chief Operating Officer at Altis Semiconductor.

The appointment of Francis Taroni reflects the desire of Soitec to further strengthen its management team whilst the group pursues its development strategy in electronics as well as in the promising area of large-scale power supply.

"We are delighted to welcome a high class executive like Francis Taroni into our group. With his successful international back-

ground and his in-depth knowledge of the industry, he will bring the experience and vision we need to deploy our industrial strategy, supporting the demands of our clients and the growing needs of the market," said Paul Boudre, Soitec's Chief Operating Officer.

[Source: Soitec]



EUROSIO Network

Thematic network on silicon on insulator technology, devices and circuits.

If you want to contribute to the EUROSIO Newsletter, you can email us with any outstanding event, announcement or news

Mail: eurosoi@ugr.es

The **EUROSIO** network embraces a broad range of research areas related to **Silicon-On-Insulator** technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). **EUROSIO** aims at federating the existing research work on **SOI** topics and at providing an appropriate communication channel between academic groups and industrial production centres.

CALENDAR

- ESSDERC ESSCRIC 2010

Sevilla, Spain.

September 13th-17th, 2010

- FDSOI Workshop

Tokio, Japan

September 25th, 2010

- 2010 IEEE International SOI Conference

San Diego, California (USA)

October 11th-14th, 2010

- 218 ECS Meeting

Las Vegas, Nevada (USA)

October 10th-15th, 2010

- EUROSIO 2011 Workshop

Granada, Spain

January 17th-19th, 2011

- CDE 2011

Palma de Mallorca, Spain

February 8th-11th, 2011

- Ultimate Integration on Silicon Conference (ULIS)

Cork, Ireland

March 14th-16th, 2011

- 219 ECS Meeting

Montreal (Canada)

May 1st-6th, 2011