

THEMATIC NETWORK  
ON SILICON ON  
INSULATOR  
TECHNOLOGY,  
DEVICES AND  
CIRCUITS.



# EUROSIO

# Newsletter

VOLUME I

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## EDITORIAL



**Francisco Gámiz**  
Professor  
Univ. Granada (Spain)

Ten years ago, Prof. Sorin Cristoloveanu provided me with the opportunity to convene the European Silicon-on-Insulator community in Granada. That was the beginning of a very long friendship. As a tireless scientist, a great pioneer and a man with a view to the future, Prof. Cristoloveanu thought it was the right moment to do something about SOI. Silicon bulk technology was approaching its limits and SOI technology was identified by the International Semiconductor Industry as a good candidate for the following years. Wide-ranging efforts to research this technology had been made since the sixties in labs all over Europe, even when it was thought that SOI technology was no more than a niche for some romantic and over-optimistic "troubadours".

With the city of Granada and its Alhambra palace as witnesses, we organised, in October 2000, a rather informal and lively meeting, the main objective of which was to discuss the place of SOI technology in Europe. Many key players in the European SOI scene have joined us since then: Prof. Denis Flandre, Prof. Cor Claeys, Prof. Jean-Pierre Colinge, Dr. Carlos Mazuré and many others. It was the first time the word EUROSIO entered our minds. After two days of fruitful discussion, the following conclusions were drawn: a) The posi-

tion of European industry with regard to SOI/SOS technology was weak, in spite of the fact that more than 20 research groups (from academia and research labs all over Europe) were successfully working on SOI technology with a very broad scope, from materials to final user applications; b) The main reason for this was the wide gap between industry and research centres with regard to SOI; c) There existed many commercial applications (RF, wireless communications, high temperature, etc.) where European industry could have a dominant position if the appropriate technology were provided. d) It was necessary to take advantage of the previous experience of research groups and to join forces to maximise the synergy between individual skills, thus achieving the best global results.

In order to improve the situation, it was necessary to work towards a European initiative aimed at organising the existing

research work on SOI topics and supporting all the actions that might guide the European semiconductor industry to a dominant position in SOI-based applications. This was the birth of the EUROSIO network, with the sponsorship and support of the European Commission.

Now, after several years of intense work and networking, the situation is different to that of those early days. In 2003, the European Commission supported the creation of a European Network on Silicon on Insulator Technology, Devices and Circuits, whose main goal was to create a discussion forum for the exchange of ideas and results on the topic of Silicon-On-Insulator technologies in Europe, and to facilitate the synergy between research groups which would enable the use of Silicon-On-Insulator (SOI) technology as an effective tool to push the limits of CMOS and prepare for post-CMOS.

*(continues on page 4)*

## ANNOUNCEMENT

**EUROSIO+ fundings for exchanges aimed at scientists in order to enhance collaborations and information exchange.**

EUROSIO+ will fund exchanges in terms of travelling and research visits for scientists (students and senior scientists) in order to enhance collaborations and information exchange. Priority will be given to visits involving an industrial partner to allow a better integration of the European industry in the Network.

Applications must be received

before June 15th, including a short CV, an invitation letter from the institution to be visited and a comprehensive description of the visit (purpose, destination, duration, budget, etc). Further information can be found at the EUROSIO web site <http://www.eurosoi.org>.

## NEWS

## Emerging materials on the Roadmap for silicon-based IC systems

Table 1. Emerging materials status\*

Emerging material	First year coverage	Chip products on market	Close to mainstream acceptance	Change of importance since 2005		
				Increased	No change	Decreased
Global strained Si	2003	No	No			•
Global strained SOI	2003	No	No	•		
Germanium channel transistors	2003	No	No	•		
III-V channel transistors	2007	No	No			N/A
Isotopically pure Si	2003	No	No			•
Silicon on diamond	2005	No	No			•
Silicon on SiC	2005	No	No			•
Silicon on alumina	2005	No	No			•
Channel orientation	2005	Yes	Yes	•		
Surface orientation	2005	No	No			•
Carbon nanotubes	2005	No	No			•
High resistivity Si	2003	Yes	Yes	•		
Optical interconnection on Si	2003	No	No			•
Phase change memory	2007	No	No			N/A

\*Using the technologies that have been covered by the ITRS Emerging Materials committee since its inception in 2003, along with several status columns.

## Emerging materials status

*“The latest chips will make it easier for system designers to use their existing AM2 board designs for single core chips”, AMD said.*

In general, emerging materials will augment silicon transistor technology by providing enhanced speed, lower-power consumption, improved heat dissipation, improved memory capacity/data retention, or added RF/analog functionality while maintaining the large scale integration capability of CMOS. The augmentation of the silicon starting material need not be entirely silicon-based as long as CMOS system improvement is the end goal. As an example, the integration of III-V compound optoelectronics on silicon (Si) for en-

hanced bandwidth for I/O-limited CMOS technologies would be considered an emerging material application.

The definition of emerging materials is as follows: novel starting materials, structures, and processing methodologies that will enable anticipated roadmap requirements and enhance silicon-based CMOS technology.

The International Technology Roadmap for Semiconductors (ITRS) Emer-

ging Materials Committee has now tracked technologies for close to four years. In that time, some technologies have demonstrated progress towards mainstream applications (i.e., have moved beyond ‘emerging’ status); some technologies have continued to stay active but have not moved into mainstream applications; and some technologies have shown some loss of momentum.

[Source: Solid State Technology]

## NEWS

## AMD unveils three chips for embedded systems

Advanced Micro Devices has launched three dual-core processors for embedded systems that span entry-level networked storage systems to telecommunication products, digital signage, and point-of-sale, gaming, and kiosk systems.

The AMD Athlon X2 dual-core processors, models 3400e, 3600+, and 4200+, run at low-power envelopes of 22 watts for the 3400e and 35 watts for the other two pro-

ducts. The latest chips are AM2 socket-compatible, which will make it easier for system designers to use their existing AM2 board designs for single-core chips, AMD said.

The processors are designed to be paired with the AMD M690E chipset. They also can be combined with Broadcom chipsets, including the HT-2100 and HT-1000. The new products are expected to ship in the second quarter and will

have a five-year life cycle.

Along with the new chips, AMD unveiled a reference design kit for the Storage Bridge Bay 2.0 specification based on the AMD Athlon processor. The SBB defines mechanical, electrical, and low-level enclosure management requirements for a slot that supports storage controllers from a variety of independent hardware and system vendors.

[Source: EE Times]

## NEWS

## AMD Launches World’s First x86 Triple-Core Processors

AMD announced the availability of AMD Phenom™ X3 8000 series triple-core processors, providing gamers and digital media enthusiasts with exceptional performance at mainstream price points. AMD Phenom X3 processors are designed to improve multi-threaded application performance over dual-core processors at the same clock speed.

As the world’s only triple-core x86 processor, AMD Phenom X3 processors bring multi-core technology to a broader audience in search of desktop PCs that easily handle today’s digital entertainment workloads.

“In 2007, AMD committed to delivering AMD Phenom triple-core processors in Q1 2008 and today the company

makes good on that promise,” said Bob Brewer, “AMD understands that today’s PC applications are best accelerated with a range of multi-core products from quad- to triple- to dual-core processors, and that’s why we now deliver the broadest multi-core desktop lineup in the industry.”

[Source: AMD]



NEWS

Honeywell Announces New High Temperature Analog Silicon Chip for Aerospace and Deep Drilling

Operations

**Honeywell**

Honeywell announced that its Aerospace business has unveiled a new high temperature Silicon On Insulator electronic component with dual applications in the aerospace and oil industries.

The chip can withstand high temperatures and be used in aircraft engines or in deep drilling operations to enhance the nation's energy

supply. It was designed and developed as part of Honeywell's diverse suite of aerospace and industrial electronics.

"The aerospace and oil and natural gas industries each require high performance components that operate over wide temperature ranges," said Brian Link, Business Director, Honeywell Defense and Space. "Honeywell's Silicon On Insulator technology is critical for instrumentation and sensor measurements in these environments. The dual precision chip will be used in high temperature zones on jet engines for instrumentation

and control, as well as operating in temperatures up to 225 degrees C and at depths exceeding 20,000 feet in deep drilling operations.

Honeywell's high temperature electronics improve system reliability and help to reduce operators' equipment downtime and weight.

Honeywell's new high temperature dual precision operational chip model HTOP01 was developed with several industrial partners as part of the U.S. Department of Energy's Deep Trek Program.

[Source: PRNewswire]

NEWS

Timing not right for 450mm, says AMD's Grose

Speaking at The ConFab in Las Vegas, AMD's Doug Grose said that the timing is not right for a transition to 450mm wafers, and suggested that the concept of the industry historically moving to a new wafer size every ten years was flawed.

Describing the present macro-economic picture as "pretty bleak," Grose gave a nod to the cost that equipment and material suppliers must carry in making a wafer size change a reality. "Distribution of profit across our industry is really not equitable.

We all know that we can't create shareholder value without the equipment and software and materials suppliers and neither can they," Grose said. "So what sense does it really make to pursue an industry strategy that's not really a win-win for everybody? The last thing in the world we need right now is to starve our suppliers. That's obviously like shooting ourselves in the foot."

Grose estimated that 4% of the industry's 25%-20% annual gains in productivity really come from increased wafer size. The rest

comes from smaller die sizes, process improvements and obviously improved yields, defect density, etc. "The cost to the industry of driving to get that 4% a year is going to be very, very large. It seems inevitable we're going to have to make that move because the benefits are significant," he said, and asked: "But when, and how do we get the most from 450mm once we do make that move?"

[Source: Solid State Technology]

*"what sense does it really make to pursue an industry strategy that's not really a win-win for everybody?," said Grose*

EUROSOI NEWS

First Announcement of the EUROSOI Workshop 2009

A year on, as is tradition since 2005, and for the fifth consecutive time within the framework of the EUROSOI Network, a new edition of the EUROSOI Workshop will take place next January. Next year 2009 event will be held in Chalmers, Sweden.

EUROSOI Workshop is an international forum to promote interaction and exchanges between

research groups and industrial partners involved in SOI activities all over the world.

EUROSOI covers recent progress in SOI technologies and will be of interest to materials and device scientists, as well as to process, circuits and applications oriented engineers.

Complete information about the 2009 Workshop will soon be avail-

able at the EUROSOI web site <http://www.eurosoi.org>



*We are just at the beginning of this exciting stage. The challenges are many and the road not easy*

## EDITORIAL (cont.)

Today, the EUROSOI network comprises more than 30 partners from all over Europe, with expertise in all fields of SOI technology. The EUROSOI network has already made possible the achievement of a large part of this objective by successfully organising and bringing to fruition during the last three years a significant number of events such as the EUROSOI roadmap and state of the art documents, workshops, training events and scientific exchanges.

In the framework of the new FP7, a new project, EURO-SOI+ has been launched, started on January 1st 2008. The first goal of the new project is the upgrading and maintenance of this important forum, providing updated versions of the State-of-the-Art report and Roadmap, facilitating scientific exchanges between partners, organising works-

hops and later, using it as a launch-pad for other important objectives:

- To create a durable European School of SOI Technology.
- To foster and co-ordinate the initiatives and activities required to successfully face up to some of the challenges identified and listed in the EUROSOI Roadmap.
- To co-ordinate the development of a research-dedicated platform in order to address circuit design aspects, focusing on the advantages of SOI for Low Power applications. In two to three years, this platform will provide, through its integration in EURO-PRACTICE, prototyping and Multi-Project-Wafers (MPW) in SOI open to European research groups and Fabless Semiconductor companies (SMEs) using the LETI SOI process.

We are just at the beginning

of this exciting stage. The challenges are many and the road not easy, but with the help of all of you, I am sure we will be successful, and this will also mean success in rejuvenating the old Europe.

This is the first of what I hope will be a long series of EURO-SOI Newsletters. Periodically this short publication will collect brief announcements and links to advances in SOI technology all over the world. Here, you will also find the steps forward, activities and progress of our/your EURO-SOI Network, whose ultimate goal is to become an open platform for all our people, the SOI people. To this end, I sincerely invite all of you to contribute in developing this publication.

I wish you an interesting and fruitful SOI adventure. Good luck.

## NEWS

### IBM Unveils Three Energy-Efficient Servers Powered by Quad-Core AMD

#### Opteron™ Processors

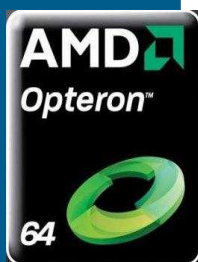
AMD announced growing industry support for the Quad-Core AMD Opteron™ processor among global OEMs continues with IBM's launch of three updated System x™ servers. Designed to address customer priorities such as energy efficiency, performance, scalability, and virtualization, the Quad-Core AMD Opteron processor-based servers from IBM offer an exceptional power-efficient platform for today's most demanding datacenters.

"Quad-Core AMD Opteron processor-based servers deliver energy-efficiency even in

the context of satisfying IBM's most demanding high-performance computing solutions," said Randy Allen, senior vice president, Computing Solutions Group, AMD. "Datacenter managers are increasingly seeking a balance of performance, energy-efficiency, and advanced virtualization functionality in order to optimize server resources amidst skyrocketing power, cooling and space costs. The Quad-Core AMD Opteron processor is at the forefront of addressing this new real-world definition of datacenter performance."

"IBM continues to deliver innovation and choice in the x86 market with today's introduction of System x servers based on AMD's new Quad-Core processors," said James Northington, vice president, IBM System x. "The new System x3755 allows clients to grow the system along with their business, affordably scaling from the standard 2 socket system to 3 and 4 socket configurations while delivering industry leading price and performance."

[Source: AMD]





## EUROSIO Network

**Thematic network on silicon on insulator technology, devices and circuits.**

Mail: [eurosoi@ugr.es](mailto:eurosoi@ugr.es)

The **EUROSIO** network embraces a broad range of research areas related to **Silicon-On-Insulator** technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space). **EUROSIO** aims at federating the existing research work on **SOI** topics and at providing an appropriate communication channel between academic groups and industrial production centres.

## CALENDAR

**- MIGAS International Summer School**

Autrans-Grenoble, France.

June 28th - July 4th, 2008

**- 2008 IEEE International SOI Conference**

Hudson River Valley

New York, USA

October 6th - 9th, 2008

**- European School On Nanosciences & Nanotechnologies**

Grenoble, France.

August 24th - September 13th, 2008

**- Third SINANO Device Modeling Summer School**

Bertinoro, Italy.

September 1st - 5th, 2008

**- 38th European Solid State Device Research Conference and 34th European Solid State Circuits Conference**

Edinburgh, United Kingdom.

September 15th - 19th, 2008