



Thematic Network on Silicon on Insulator Technology, Devices and Circuits.  
[IST-1-506653-CA]

## EUROSIO "Who is Who" Guide

### *Name of the organisation*

<i>Organization Legal name:</i>	<b>Politecnico di Torino</b>
<i>Organization short name:</i>	Polito
<i>Internet homepage:</i>	<b>www.polito.it</b>

### *Contact person*

<i>Name:</i>	<i>Casu</i>	<i>Title:</i>	<i>Dr.</i>
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<i>Postal Address</i>	<i>Politecnico di Torino, Dipartimento di Elettronica C.so Duca degli Abruzzi 24, I-10129 Torino, Italy</i>		

### **Other Senior Researchers:** (up to 10 names, please include e-mail address)

Dr. Mariagrazia Graziano, [mariagrazia.graziano@polito.it](mailto:mariagrazia.graziano@polito.it)

Prof. Gianluca Piccinini, [gianluca.piccinini@polito.it](mailto:gianluca.piccinini@polito.it)

Prof. Maurizio Zamboni, [maurizio.zamboni@polito.it](mailto:maurizio.zamboni@polito.it)

Prof. Guido Masera, [guido.masera@polito.it](mailto:guido.masera@polito.it)

### **Experience and expertise fields:** (50 words)

**Design of digital Application Specific Integrated Circuits (ASIC) in CMOS Bulk and SOI; Low-power SOI SRAM design; SOI DTMOS and other body-biasing schemes; High-speed SOI domino logic; Modelling of SOI behaviour in digital circuits (Partially and Fully Depleted); Performance trend predictions for future SOI and Bulk CMOS technologies.**

### **Facilities and Equipment:**

**SUN Solaris and PC Workstations fully equipped for ASIC design with up-to-date EDA tools (front-end to back-end: Mentor, Synopsys, Hspice, Eldo, Cadence) and design-kits of CMOS Bulk and SOI technologies;**

**High-end Xilinx FPGA boards for prototyping;**

**Testing machine for packaged chips;**

**High-speed digital oscilloscopes;**

### **Three last international research projects:**